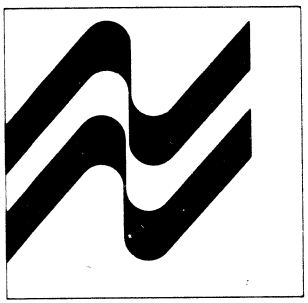
PROM/EPROM MEMORY DATABOOK

NATIONAL SEMICONDUCTOR



National Semiconductor

BIPOLAR PROMS 1

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National Semiconductor Corporation

National Semiconductor Corporation was founded in 1959 in Danbury, Connecticut as an electronic component supplier. With corporate offices now in Santa Clara, California and under the leadership of one of the industry's strongest management teams, National has grown from a component and custom circuit supplier with sales of $5.3 million in 1965 to a diversified company with sales of $325 million in 1976.

Products

Now the second-largest semiconductor supplier in the world, National produces a large volume of standard and custom integrated circuits and a broad line of electronic products for the consumer, commercial, industrial and OEM markets. In addition to the memory systems described in this brochure, National produces supermarket electronic cash register systems, consumer electronic products, microcomputers, and IBM-software-compatible CPU replacements for 370 computer systems.

Facilities and Offices

Including 350,000 square feet in the Santa Clara world headquarters, additional facilities in Danbury, Connecticut, and West Jordon, Utah, and off-shore production plants in eight foreign countries, National has assembly and test facilities totaling 700,000 square feet. National products are represented by a world-wide sales network with offices in the United States, Canada, Europe, Australia and the Orient.

Ordering Information

All products may be ordered through a franchised National distributor or through an National sales representative. (See page)

New Products

"New products" listed in this book are devices which National plans to introduce in the first half of 1978. The devices are not available from stock. Status information can be obtained upon request.

Programming Input Formats

National can programm your PROM or ROM from any of the following inputs: thruth table, paper tapes, and punched cards.

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BIPOLAR PROM CROSS REFERENCE GUIDE

Size	Organ.	Pin	Tech.	Outp.	AMD	Fair-child	Harris	Fujitsu	Intel	Intersil	MMI	Motorola	**National**	NEC	Sescosem	Ray-theon	Signetics	T.I.
256	32x8	16	S-TTL	OC	AM29750DC AM27S08DC		HM7602	MB7056		IM5600	6330-1		**54S188** **74S188**				X82S23n	SN74S188N
				TS	AM29751DC AM27S09DC		HM7603	MB7051		IM5610	6331-1		**54S288** **74S288**				X82S123n	SN74S288N
256	32x8		ECL	OE								10139*					10139*	
512	64x8	24	S-TTL	OC			HPROM05/2*											
512	64x8	24	TTL	OC								5303A* 5003A* 5304A* 5004A*						SN74186*
1024	256x4	16	S-TTL	OC	AM29760DC AM27S10DC	93417	HM-7610 HM-7610A	MB7057	d3601	IM5603	6300-1		**54S387** **74S387**	μPB403D*	SFC71301AE*	29600*	X82S126	SN74S387N
				TS	AM29761DC AM27S11DC	93427	HM-7611 HM-7611A	MB7052	d3621a d3602a*	IM5623	6301-1		**54S287** **74S287**		SFC7130E*	29601*	X82S129	SN74S287N
1024	256x4	16	TTL	OC													82S27* 82S129*	
				TS													82S129*	
1024	256x4	16	ECL	OE		10416* 100416*						10149*					10149* GxB10149*	
1024	256x4	16	CMOS	OC/TS			HM-661*											
2048	512x4	16	S-TTL	OC	AM27S12 AM29770	93436	HM-7620 HM-7620A*	MB7058	d3602 d3602a-2*	IM5604	6305-1		**54S570** **74S570**					
				TS	AM27S13 AM29771	93446	HM-7621 HM-7621A*	MB7053	d3622 d3622a* d3622a-2*	IM5624	6306-1		**54S571** **74S571**					

* NOT NECESSARILY PIN COMPATIBLE

Size	Organ.	Pin	Tech.	Outp.	AMD	Fair-child	Harris	Fujitsu	Intel	Intersil	MMI	Motorola	**National**	NEC	Sescosem	Ray-theon	Signetics	T.I.
2048	256x8	20	S-TTL	OC							6308-1*					29660*		SN74S470N*
				TS							6309-1*					29661*		SN74S471N*
2048	256x8	24	S-TTL	OC							6335-1*							
				TS							6336-1* 63135-1*							
2048	256x8	24	TTL	TS													82S114n*	
2048	512x4	16	TTL	OC								7620*					82S130n	
				TS								7621*					82S131n	
4096	512x8	24	S-TTL	OC		93438	HM7640 HM7640A* HM7640AR* HM7646R*		md3604 d36041-6* d3604a/a-2* d3604/a/* d3604-4*	IM5605	6340-1		**54S475** **74S475**	µPB405D*				SN74S475N
				TS		93448	HM7641		d3624 d3624a* d3624a-2*	IM5625	6341-1 63137-1* 63139-1* 63141-1*		**54S474** **74S474**	µPB425D*				SN74S474N
4096	512x8	20	S-TTL	OC			HM7648*				6348-1		**54S473** **74S473**					SN74S473N
				TS			HM7649*				6349-1		**54S472** **74S472**					SN74S472N
4096	1024x4	18	S-TTL	OC		93452	HM-7642	MB7059	d3605 d3605-2*		6352-1 6350-1*		**54S572** **74S572**	µPB406D*				
				TS		93453	HM-7643	MB7054	d3625		6353-1		**54S573** **74S573**	µPB426D*				
4096	1024x4	16	S-TTL	OC			HM-7644*		d3625-2*									
4096	512x8	24	TTL	OC								7640*					82S140n	
				TS								7641*					82S115n 82S141n	

* NOT NECESSARLY PIN COMPATIBLE

BIPOLAR PROM CROSS REFERENCE GUIDE

Size	Organ.	Pin	Tech.	Outp.	AMD	Fair-child	Harris	Fujitsu	Intel	Intersil	MMI	Motorola	**National**	NEC	Sescosem	Ray-theon	Signetics	TI
4096	1024x4	18	TTL	OC								7642/3/4					82S136	
				TS													82S137	
8192	1024x8	24	S-TTL	OC		93450*	HM7680 HM7680R*	MB7055*	d3608 d3608 – 4*		6380-1 (LS) 6384-1 (LS)*							
				TS		93451*	HM7681 HM7681P* HM7681RP*	MB7060*	d3628 d3628-4*		6381-1 (LS) 6385-1 (LS)*			μPB427D				
8192	2048x4	18	S-TTL	OC			HM7684* HM7684P*				63100-1 (LS)		**54S672**					
				TS			HM7685* HM7685P*				63101-1 (LS)		**54S673**					
8192	1024x8	24	TTL	OC								8080* 82707* 8081* 82708*					82S180 82S181 82S2708	
8192	1024x8	22	TTL	OC							6386-1 (LS)*							
				TS							6387-1 (LS)*							
8192	2048x4	24	TTL	OC													82S184	
				TS													82S185	
8192	2048x4	20	S-TTL	OC			HM7686* HM7686N* HM7686P* HM7686RP*											
				TS			HM7687* HM7687N* HM7687P* HM7687RP*											
16384	2048x8	24	TTL	OC													82S190*	
				TS													82S191*	

* NOT NECESSARLY PIN COMPATIBLE

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EPROM CROSS REFERENCE GUIDE

	National	AMD	AMI	Electronic Arrays	Fairchild	Hitachi	Fujitsu	Intel	Intersil	Mostek	Motorola	RCA	Sescosem	SGS-Ates	Signetics	TI	Toshiba
8192 (1024 x 8) 24 pin	**2708Q**	AM2708		EA2708	2708 2708-1	HN462708	MB8518E MB8548H	b2708 b2708-1 mc2708 b2758	D2708	MK2708	2708L 27A08L 68708L 68A708L		SFF1708AK	M2708	2708	TMS2708JL TMS27L08JL	TMM322C
2048 (256 x 8) 24 pin	**1702AQ** **5203**	C1702A-1 AM1702ADC AM1702AL-1				HN351702A		b1702a b1702a-2 b1702a-6 b1702a1 b1702a1-2 mc1702a		MK1702-1 MK1702-2 MK1702-3		CPD1842	SFF7702AK		1702A		TMM121C TMM121C-1
(512 x 4)	**4203**																
4096 (512 x 8) 24 pin	**5204** **4204** **5204-1**		S5204A S6834														
16384 (2048 x 8) 24 pin	**2716**			EA2716				b2716			2716 2717					TMS25/6	
4096 (512 x 8) 24 pin				EA2704				b2704						M2704	2704		

* NOT NECESSARLY PIN COMPATIBLE

EPROM CROSS REFERENCE GUIDE

1. BIPOLAR PROMS

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Bipolar PROMs

- Titanium-Tungsten (Ti-W) Fuses
- Schottky-Clamped for High Speed
- PNP Inputs for Reduced Input Loading
- All Parameters Guaranteed over Temperature
- Low Voltage Tri-Safe™ Programming
- Generic Card Programming

The use of titanium-tungsten (Ti-W) as a 'buffer' material between the aluminum interconnect and the platinum-silicide 'barrier' is a standard of the Schottky Bipolar process metalization system. (Refer to Figure 1)

Utilizing titanium-tungsten as a fuse metal therefore 'uncomplicates' the metallic structure of these Bipolar PROMS.

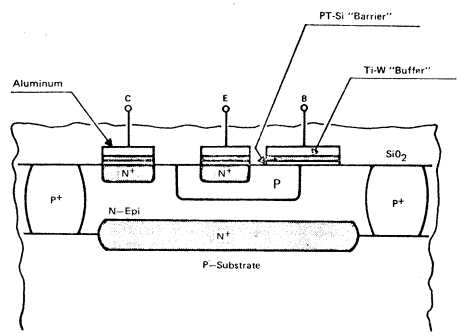
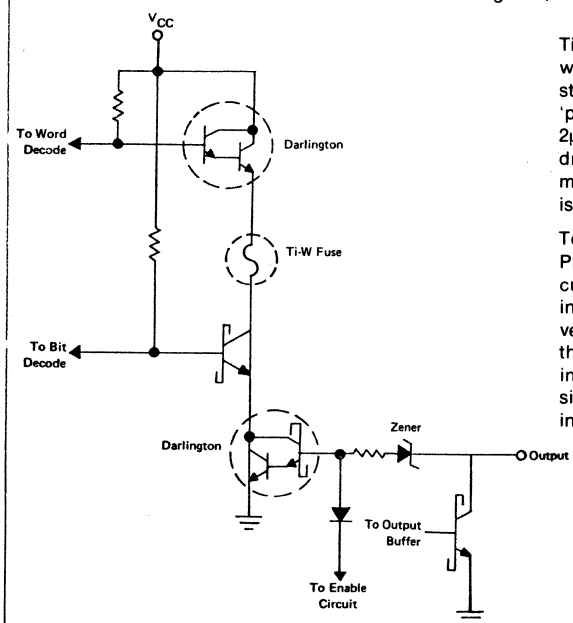


Figure 1



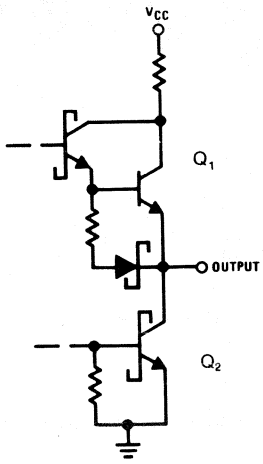
Titanium-tungsten has many desireable properties which make it a preferable fuse material. It is extremely stable metal which does not oxidize readily and is very 'processable'. Thus, fuses of uniform size (NOM: 2μ x IKÅ) and resistivity are readily produced. The one drawback of Ti-W as a fuse material is its extremely high melting temperature (3300 °C). A very high energy pulse is required to open the fuse.

To insure reliable programming, National's Ti-W PROMS incorporate the Darlington programming circuit shown in Figure 2. This circuit 'pulse shapes' the input from the programmer and provides a high energy very fast current pulse to the selected fuse. Because of the speed of this on-the-chip approach localized heating is minimized. This results in a wide gap free of residual material, and as demonstrated by the data herein, excellent reliability.

TRI-STATE OUTPUT VS. OPEN COLLECTOR OUTPUT

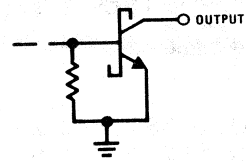
The TRI-STATE output offers two advantages over Open Collector types. The first advantage is that a low impedance driver, Q_2, is available for driving capacitance on the memory output, resulting in faster low to high transition. The second advantage is that no pullup resistor is required. When the chip enable is active either Q_1 or Q_2 is on, depending upon the data in the memory array. When the chip enable is not active Q_1 and Q_2 are off, permitting wire ORing of memory outputs. This condition is called the high impedance TRI-STATE.

Typical TRI-STATE Output



In a system environment, up to 21 outputs of the commercial device or 10 outputs of the military device can be connected to a common bus. All of the devices except one are placed in the high impedance state and selected device is enabled and has the characteristics of a TTL totem pole output. The user should avoid having more than one device enabled on the bus at one time since the enabled device will deliver its short circuit current into the other enabled device(s). While physical damage to the device under these circumstances is unlikely, system noise problems could result.

Typical Open-Collector Output



BIPOLAR PROM/ROM SELECTION GUIDE

Organ.	Size	Pack Pins	Prom. Part No.	Outp.	Temp.	Max T_{AA}	Max T_{EA}	Max T_{ER}	Max I_{CC}	Interchangeable Rom
						n sec				
256	32 x 8 (high speed)	J 16	54S188	OC	C	40	30	30	110	DM5488
		J	54S288	TS		40	30	30	110	DM5498
		N, N	74S188	OC		30	20	20	110	DM7488
		N, J	74S288	TS		30	20	20	110	DM7498
1024	256 x 4 (high speed)	J 16	54S387	OC		60	30	30	130	DM54S187
		J	54S287	TS		60	30	30	130	DM75S97
		N, J	74S387	OC		50	25	25	130	DM74S187
		N, J	74S287	TS		50	25	25	130	DM85S97
4096	512 x 8 (high)	J 20	54S473	OC		80	55	55	165	
		J	54S472	TS		80	55	55	165	
		J	74S473	OC		65	40	40	165	
		N J	74S472	TS		65	40	40	165	
2048	512 x 4 (high speed)	J 16	54S570	OC		65	35	35	130	DM54S270
		J	54S571	TS		65	35	35	130	DM54S370
		J	74S570	OC		55	30	30	130	DM74S270
		N J	74S571	TS		55	30	30	130	DM74S370
4096	1K x 4 (high speed)	J 18	54S572	OC		75	45	45	140	
		J	54S573	TS		75	45	45	140	
		J	74S572	OC		40	25	25	140	
		N J	74S573	TS		40	25	25	140	
4096	1K x 4	J 18	54S574							
		J	74S574							
4096	512 x 8 (high speed)	J 24	54S475	OC		75	40	40	170	DM77S95
		J	54S474	TS		75	40	40	170	DM77S96
		J	74S475	OC		65	35	35	170	DM87S95
		N J	74S475	TS		65	35	35	170	DM87S96

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Bipolar PROMs

DM54S188/DM74S188 open-collector 256-bit PROM
DM54S288/DM74S288 TRI-STATE® 256-bit PROM

general description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as ROM's as well as PROM's.

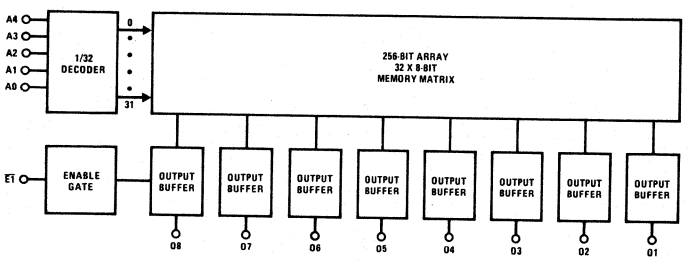
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—30 ns max
  Enable access—20 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming

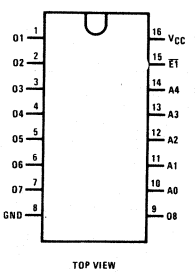
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N, J
DM74S288		X		X	N, J
DM54S188	X		X		J
DM54S288	X			X	J

block diagram



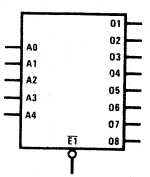
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	-0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S188, DM54S288	4.5	5.5	V
DM74S188, DM74S288	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S188, DM54S288	−55	+125	°C
DM74S188, DM74S288	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S188, 54S288			DM74S188, 74S288			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		70	110		70	110	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20	−45	−70	−20	−45	−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S188, 54S288 5V ±10%; −55°C to +125°C			DM74S188, 74S288 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			22	40		22	30	ns
t_{EA}	Enable Access Time			15	30		15	20	ns
t_{ER}	Enable Recovery Time			15	30		15	20	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to either A0 (pin 10) or A4 (pin 14).

National Semiconductor

Bipolar PROMs

DM54S287/DM74S287 TRI-STATE® 1024-bit PROM
DM54S387/DM74S387 open-collector 1024-bit PROM

general description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

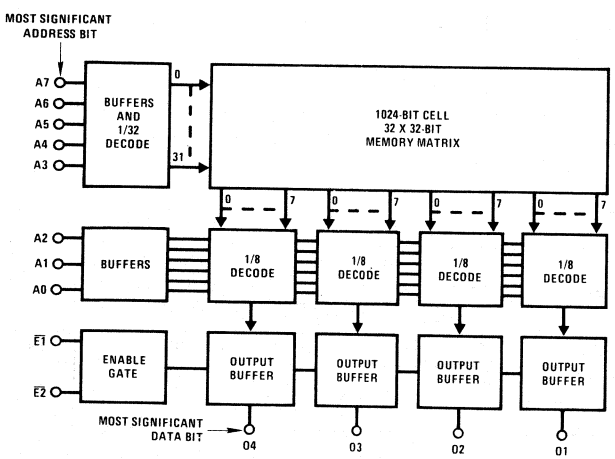
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—50 ns max
  Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S187 and DM85S97

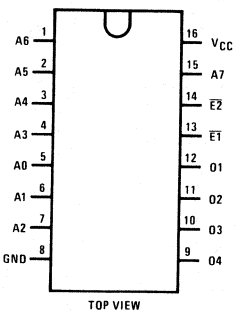
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N, J
DM74S287		X		X	N, J
DM54S387	X		X		J
DM54S287	X			X	J

block diagram



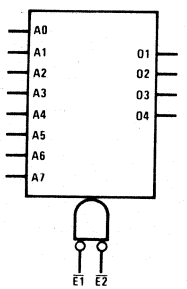
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S387, DM54S287	4.5	5.5	V
DM74S387, DM74S287	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S387, DM54S287	−55	+125	°C
DM74S387, DM74S287	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S387/287			DM74S387/287			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S387/287 5V ±10%; −55°C to +125°C			DM74S387/287 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*	10	35	60	10	35	50	ns
t_{EA}	Enable Access Time	*(Figure 2)*	5	15	30	5	15	25	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*	5	15	30	5	15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

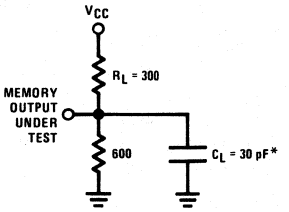
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH} or I_{CEX} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

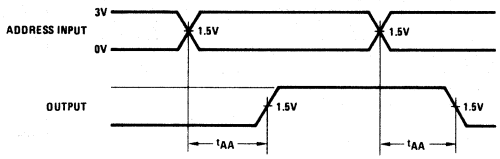


FIGURE 1. Address Access Time

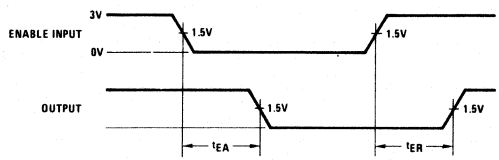
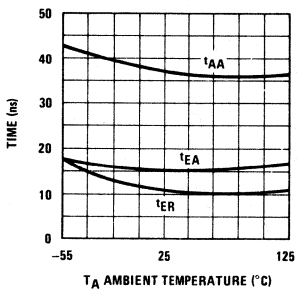


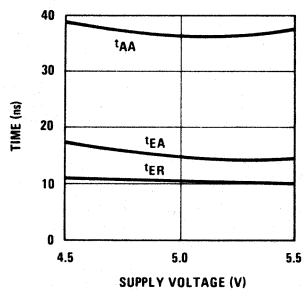
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

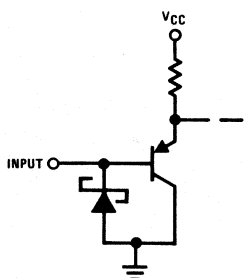


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

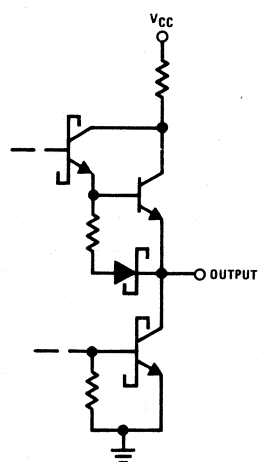


equivalent circuits

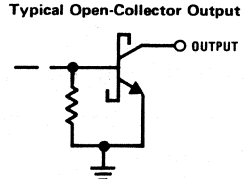
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

Bipolar PROMs

DM54S473/DM74S473 open-collector 4096-bit PROM
DM54S472/DM74S472 TRI-STATE® 4096-bit PROM

general description

These Schottky PROM memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions.

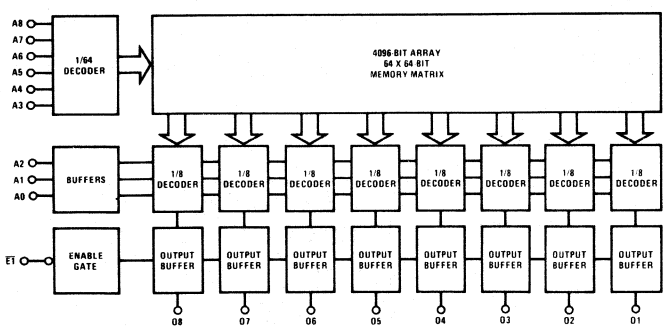
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns max
  Enable access—40 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 20-pin package

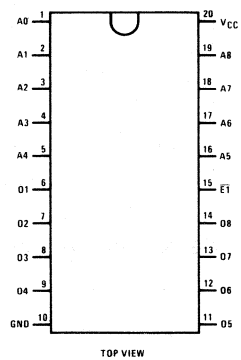
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S473		X	X		N, J
DM74S472		X		X	N, J
DM54S473	X		X		J
DM54S472	X			X	J

block diagram



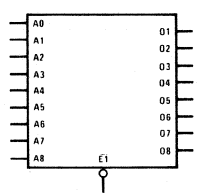
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S473, DM54S472	4.5	5.5	V
DM74S473, DM74S472	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S473, DM54S472	−55	+125	°C
DM74S473, DM74S472	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S473, 54S472			DM74S473, 74S472			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		135	165		135	165	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20	−45	−70	−20	−45	−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S473, 54S472 5V ±10%; −55°C to +125°C			DM74S473, 74S472 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			45	80		45	65	ns
t_{EA}	Enable Access Time			28	55		28	40	ns
t_{ER}	Enable Recovery Time			28	55		28	40	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V.

National Semiconductor

Bipolar PROMs

DM54S570/DM74S570 open-collector 2048-bit PROM
DM54S571/DM74S571 TRI-STATE® 2048-bit PROM

general description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

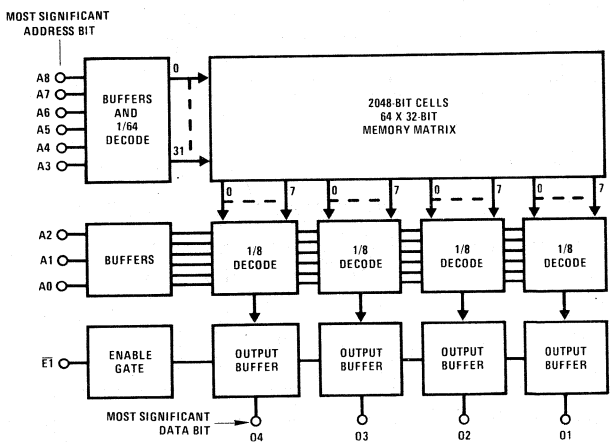
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

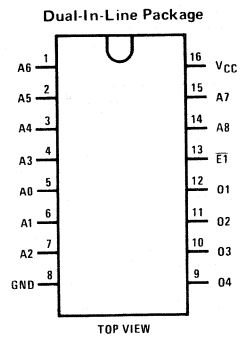
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

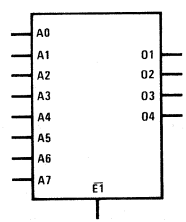
block diagram



connection diagram



logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S570, DM54S571	−55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		90	130		90	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S570, 54S571 5V ±10%; −55°C to +125°C			DM74S570, 74S571 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	65		40	55	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	35		20	30	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	35		20	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

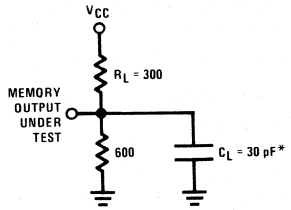
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A8 and A2 (pin 14 and pin 7).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

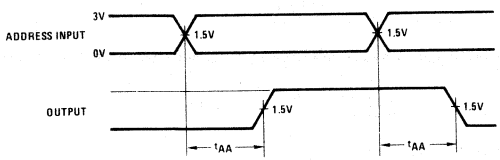


FIGURE 1. Address Access Time

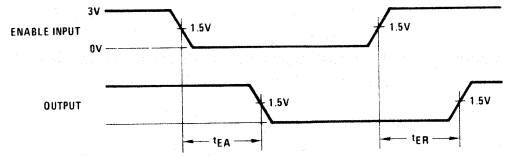
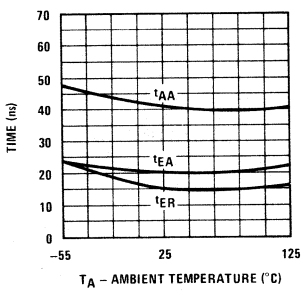


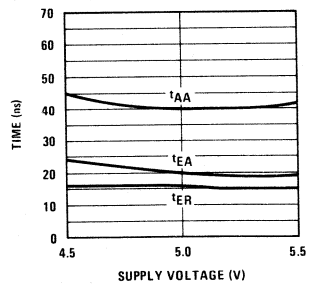
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

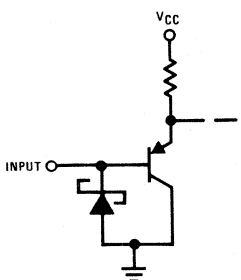


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

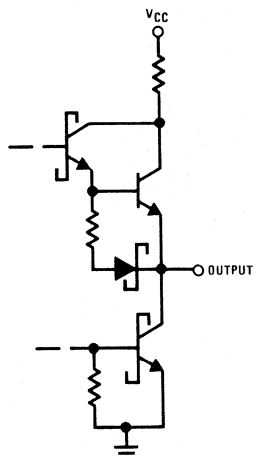


equivalent circuits

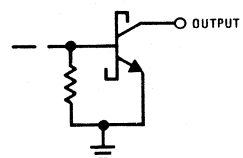
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

Bipolar PROMs

DM54S572/DM74S572 open-collector 4096-bit PROM
DM54S573/DM74S573 TRI-STATE® 4096-bit PROM

general description

These Schottky PROM memories are organized in the popular 1024 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

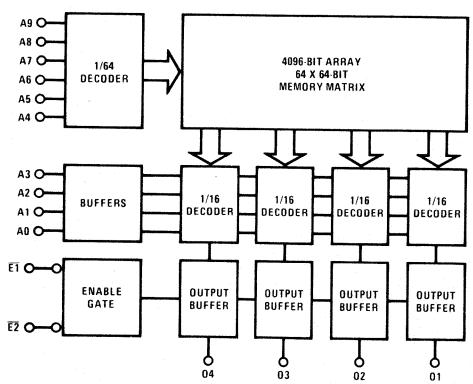
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

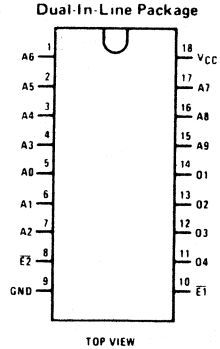
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N, J
DM74S573		X		X	N, J
DM54S572	X		X		J
DM54S573	X			X	J

block diagram



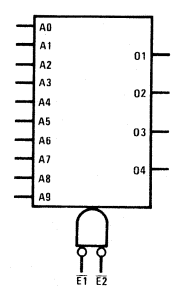
connection diagram

Dual-In-Line Package



TOP VIEW

logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S572, DM54S573	4.5	5.5	V
DM74S572, DM74S573	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S572, DM54S573	−55	+125	°C
DM74S572, DM74S573	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S572, 54S573			DM74S572, 74S573			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		125	140		125	140	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20	−45	−70	−20	−45	−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S572, 54S573 5V ±10%; −55°C to +125°C			DM74S572, 74S573 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			25	45		25	35	ns
t_{ER}	Enable Recovery Time			25	45		25	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A5 and A2 (pin 2 and pin 7).

National Semiconductor

Bipolar PROMs

DM54S574/DM74S574 TRI-STATE® 4096-bit PROM

general description

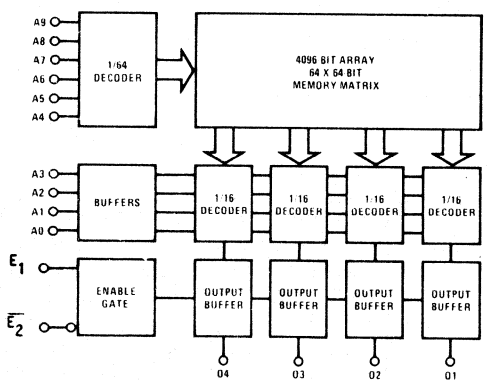
This Schottky Prom is organized in the 1024 words by 4 bit configuration. It has the same characteristics as our MM54/74S573 Prom and of course is part of Nationals Generic Prom family. The MM54/74S574 has E_1 (pin 10) high active and therefore needs E_1 high and E_2 low for selection. This pin is the R/W pin on the MM2114. This allows development of a program using our MM2114 RAM and then replacing it with this Prom.

Proms are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

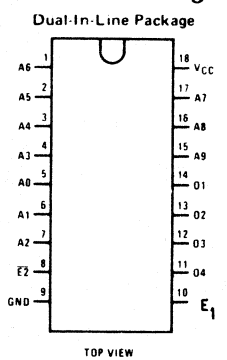
features

- Advanced titanum-tungsten (Ti-W) fuses
- MM2114 pin compatible
- Schottky clamped for high speed
  Address access-60ns max
  Enable access-35ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

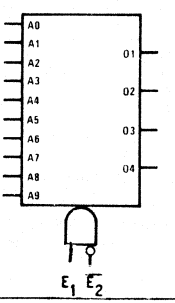
block diagram



connection diagram



logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S574	4.5	5.5	V
DM74S574	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S574	−55	+125	°C
DM74S574	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S574			DM74S574			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		125	140		125	140	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20	−45	−70	−20	−45	−70	mA
I_{HZ}	Output Leakage (TRI STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = 2 mA	2.4	3.2					V
		I_{OH} = 6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S574 5V ±10%; −55°C to +125°C			DM74S574 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			25	45		25	35	ns
t_{ER}	Enable Recovery Time			25	45		25	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A5 and A2 (pin 2 and pin 7).

National Semiconductor

Bipolar PROMs

DM54S475/DM74S475 open-collector 4096-bit PROM
DM54S474/DM74S474 TRI-STATE® 4096-bit PROM

general description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

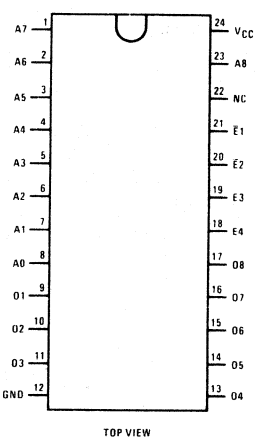
features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—65 ns
  Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S475		X	X		N, J
DM74S474		X		X	N, J
DM54S475	X		X		J
DM54S474	X			X	J

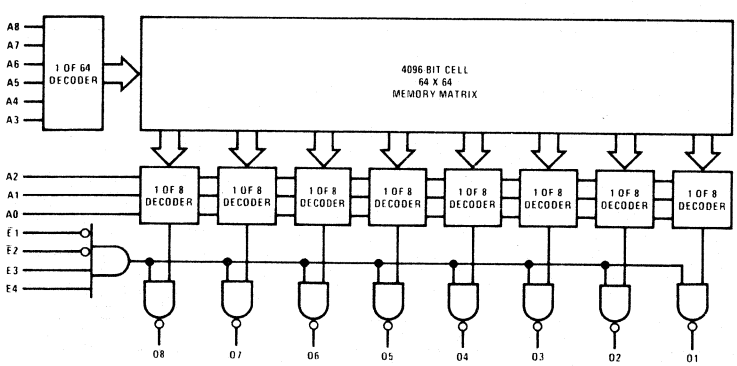
connection diagram

Dual-In-Line Package

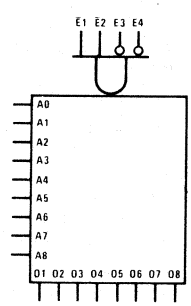


TOP VIEW

block diagram



logic symbol



absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S475, 474	4.5	5.5	V
DM74S475, 474	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S475, 474	−55	+125	°C
DM74S475, 474	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S475, 474			DM74S475, 474			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

ac electrical characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S475, 474 5V ±10%; −55°C to +125°C			DM74S475, 474 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	75		40	65	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	40		20	35	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	40		20	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

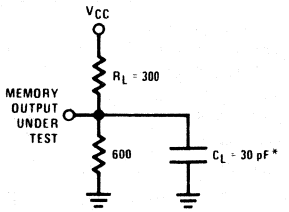
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

standard test load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

switching time waveforms

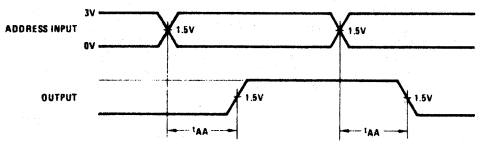


FIGURE 1. Address Access Time

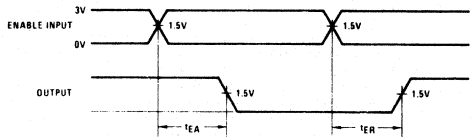
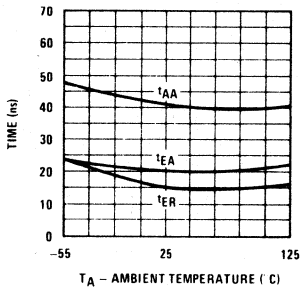


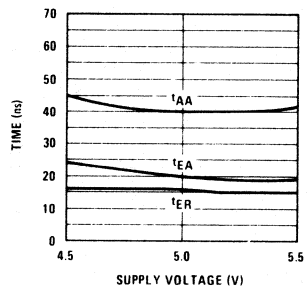
FIGURE 2. Enable Access Time and Recovery Time

typical performance characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

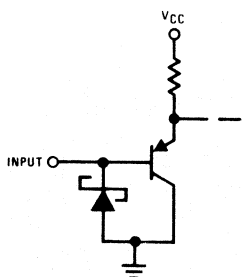


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

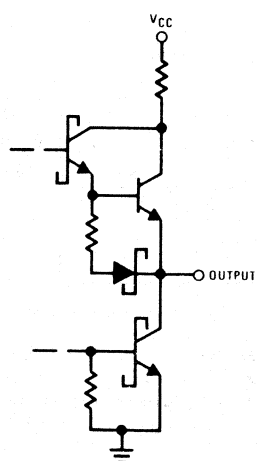


equivalent circuits

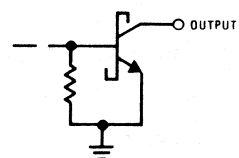
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



Programming

Commercial Programmers

Several companies make commercial programmers which will properly program National Semiconductor Proms. National Semiconductor makes it a practice to review these commercial programmers and works closely with the manufacturers to maintain a high programming yield and high reliability of programmed parts. For those customers not using an approved programmer, the programming instructions must be followed.

PROM programming procedure

These parts are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. In order to generate a high level on the outputs, the part must be programmed. Information on available programming equipment may be obtained from National. However, if it is desired to build your own programmer, the following conditions must be observed.

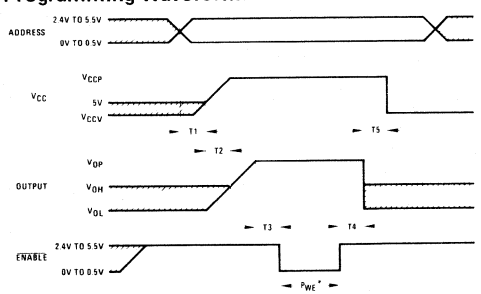
1. Programming should be attempted only at temperatures between 15°C and 30°C.
2. Addresses and chip enable pins must be driven from normal TTL logic levels during both programming and verification.
3. Programming will occur at a selected address when V_{CC} is held at 10.5V, the appropriate output is held at 10.5V and the chip is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying a high or low level to the appropriate address inputs. Disable the chip by applying a high level to one or both enable inputs.
   b) Increase V_{CC} to 10.5V ±0.5V with the rate of increase being between 1.0 and 10.0V/μs. Since V_{CC} supplies the current to program the fuse as well as the I_{CC} of the device at programming voltage, it must be capable of supplying 400 mA at 11.0V.
   c) Select the output where a high level is desired by raising that output voltage to 10.5V ±0.5V. Limit the rate of increase to a value between 1.0 and 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC} but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or tied to a high impedance source of at least 20 kΩ. (Remember that the outputs of the device are still disabled at this time because the chip enables are high.)
   d) Enable the device by taking both chip enables to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V ±0.2V. Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The chip must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c and d must be repeated 10 times or until verification that the bit has programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at programming voltage must be limited to a maximum of 25%. This is necessary to minimize chip junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled chip is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Parameters Do not test or you may program the device.

PARAMETERS		CONDITIONS	MIN	RECOMMENDED VALUE	MAX	UNITS
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V	600		750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
t_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms



T1 = 100 ns min
T2 = 5μs min (T2 may be ≥ 0 if V_{CCP} rises at the same rate or faster than V_{OP})
T3 = 100 ns min
T4 = 100 ns min
T5 = 100 ns min

*P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has programmed

2. MOS EPROMS

National Semiconductor

EPROM SELECTION GUIDE

ORGANIZATION	SIZE	PINS	EPROM PART #	OUTPUT	T_{ACC} max	T_{CO} max
256 x 8	2048	24	MM1702A	TS	1μs	900ns
1K x 8	8192	24	MM2708	TS	450ns	120ns
256 x 8 or 512 x 4	2048	24	MM4203	TS	1μs	500ns
			MM5203	TS	1μs	500ns
512 x 8	4096	24	MM4204	TS	1μs	500ns
			MM5204	TS	1.25μs	600ns
			MM5204-1	TS	700ns	500ns

National Semiconductor

MOS EPROMs

MM1702A 2048-bit electrically programmable ROM

general description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

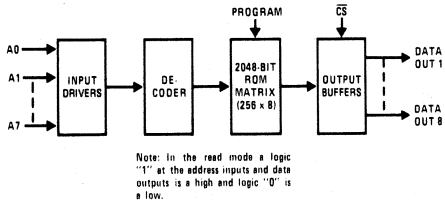
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

features

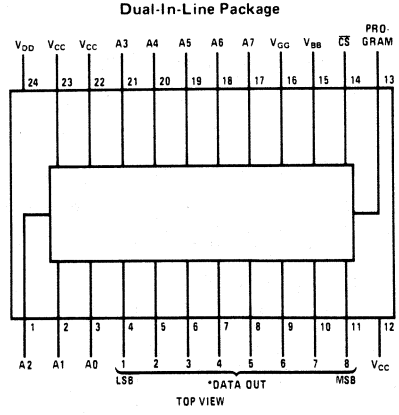
- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 x 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

block and connection diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



TOP VIEW

*This pin is the data input lead during programming.

Order Number MM1702AD
See Package 6
Order Number MM1702AQ
See Package 21

Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1–8 are pins 4–11 respectively.

absolute maximum ratings (Note 1)

Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	+0.5V to −20V
Program Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	−48V
Lead Temperature (Soldering, 10 seconds)	300°C

read operation dc characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0.0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2			1	μA
I_{DDO}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} −2 I_{OL} = 0.0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1.0, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1.0		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{OL}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V	−2.0			mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{OH}	Output High Voltage	I_{OH} = −100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DDO} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1702AL.

read operation ac characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} Set-Up (Note 1)	1			μs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{OD}	Output Deselect			300	ns
t_{OHC}	Data Out Hold in Clocked V_{GG} Mode (Note 1)			5	μs

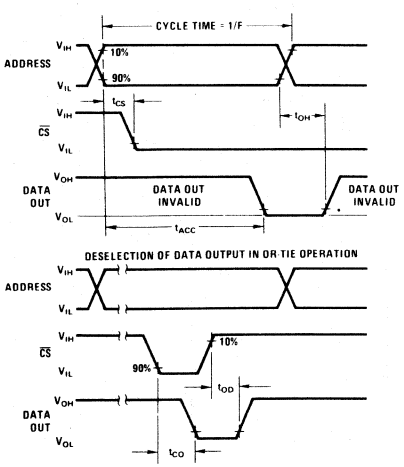
capacitance characteristics $T_A = 25°C$ (Note 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused	$V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are	$\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance (Note 1)	At ac Ground	$V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

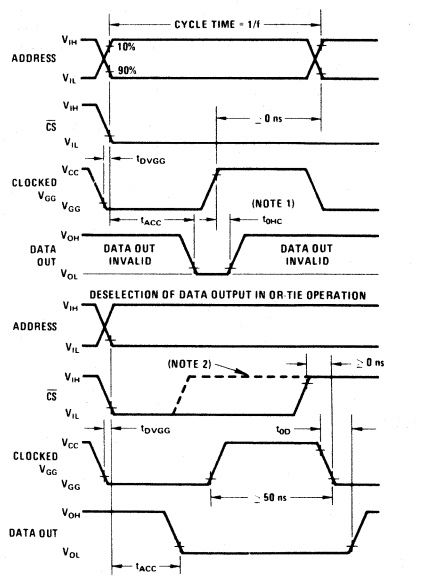
read operation switching time waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \geq 50$ ns. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \geq 15$ ns), $C_L = 15$ pF.

(b) Power-Down Option (Note 1)



Note 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

programming operation dc characteristics

T_A = 25°C, V_{CC} = 0V, V_{BB} = 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI1P}	Address and Data Input Load Current	V_{IN} = −48V			10	mA
I_{LI2P}	Program and V_{GG} Load Current	V_{IN} = −48V			10	mA
I_{BB}	V_{BB} Supply Load Current	(Note 5)		10	100	mA
I_{DDP}	Peak I_{DD} Supply Load Current	V_{DD} = V_{PROG} = −48V V_{GG} = −35V (Note 4)		200	300	mA
V_{IHP}	Input High Voltage				0.3	V
V_{IL1P}	Pulsed Data Input Low Voltage		−46		−48	V
V_{IL2P}	Address Input Low Voltage		−40		−48	V
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage		−46		−48	V
V_{IL4P}	Pulsed Input Low V_{GG} Voltage		−35		−40	V

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100μs. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100 mA max current to prevent damage to the device.

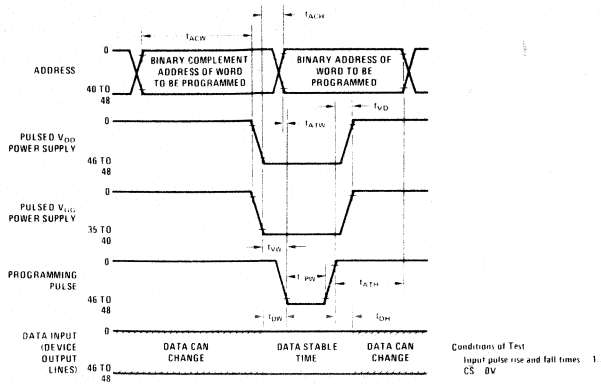
programming operation ac characteristics

T_A = 25°C, V_{CC} = 0V, V_{BB} = 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle (V_{DD}, V_{GG})				20	%
$t_{\phi PW}$	Program Pulse Width	V_{GG} = −35V, V_{DD} = V_{PROG} = −48V			3	ms
t_{DW}	Data Set-Up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{DD}, V_{GG} Set-Up		100			μs
t_{VD}	V_{DD}, V_{GG} Hold		10		100	μs
t_{ACW}	Address Complement Set-Up	(Note 6)	25			μs
t_{ACH}	Address Complement Hold	(Note 6)	25			μs
t_{ATW}	Address True Set-Up		10			μs
t_{ATH}	Address True Hold		10			μs

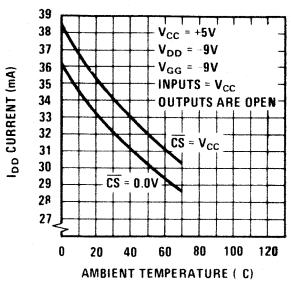
Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0–255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by x + 4x.)

programming operation switching time waveforms

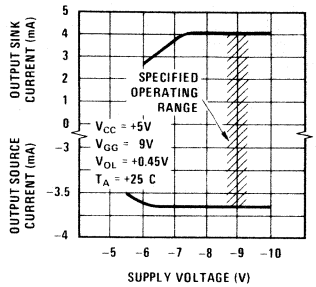


typical performance characteristics

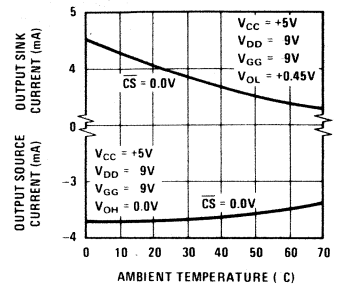
I_{DD} Current vs Temperature



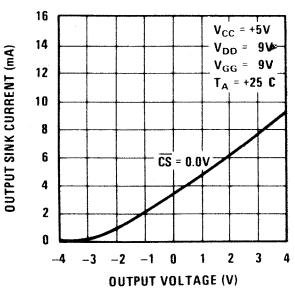
Output Current vs V_{DD} Supply Voltage



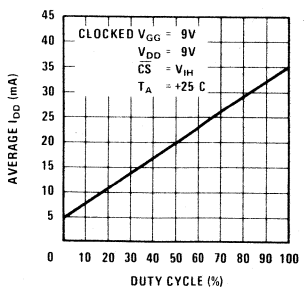
Program Waveforms



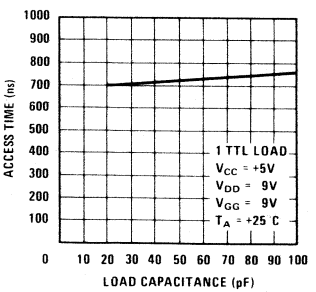
Output Sink Current vs Output Voltage



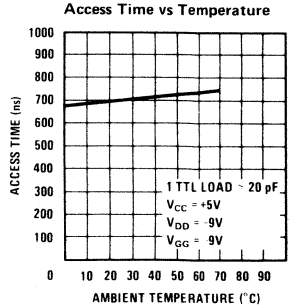
Average Current vs Duty Cycle for Clocked V_{GG} (Note 1)



Access Time vs Load Capacitance



Access Time vs Temperature



operation of the MM1702A in program mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1's" (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μs after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied. The addresses should be programmed in the sequence 0–255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (–48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 4-4). All eight bits of one word are programmed simultaneously be setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

MM1702A erasing procedure

The MM1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W sec/cm^2. Examples of ultraviolet sources which can erase the MM1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the MM1702A to be erased should be placed about one inch away from the lamp tubes. There exists no absolute rule for erase time. Establish a worst case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. (May be expressed as x + 2x.)

MM2708, 8k UV Erasable PROM

General Description

The MM2708 is a high speed 8192-bit UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

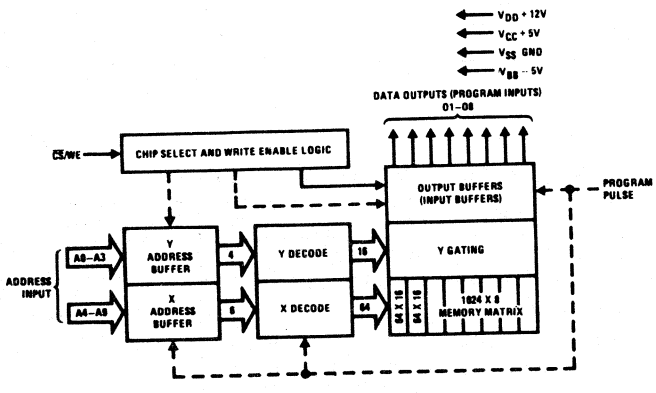
The MM2708 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

The MM2708 is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

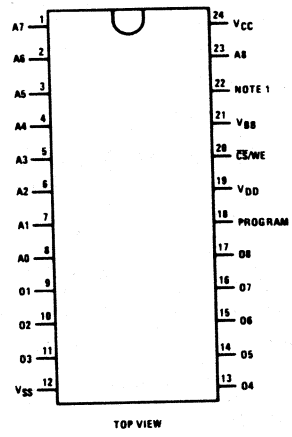
Features

- 1024 x 8 organization (MM2708)
- 800 mW max
- Low power during programming
- Access time—450 ns max
- Standard power supplies: 12V, 5V, −5V
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams



Dual-In-Line Package



MM2708: Pin 22 = A9

Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	DOUT	VSS	VSS	VDD	VIL	VBB	VCC
Program	DIN	VSS	Pulsed VIHP	VDD	VIHW	VBB	VCC

Pin Description

A0–A9	Address inputs
O1–O8	Data outputs
CS/WE	Chip select/write enable input

Printed in Germany

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} with Respect to V_{BB}	20V to −0.3V
V_{CC} and V_{SS} with Respect to V_{BB}	15V to −0.3V
All Input or Output Voltages with Respect to V_{BB} During Read	15V to −0.3V
$\overline{CS}$/WE Input with Respect to V_{BB} During Programming	20V to −0.3V
Program Input with Respect to V_{BB}	35V to −0.3V
Power Dissipation	1.5 W
Lead Temperature (Soldering, 10 seconds)	300°C

Read Operation

DC Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted, (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Sink Current	V_{IN} = 5.25V or V_{IN} = V_{IL}		1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V		1	10	μA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Voltage		V_{SS}		0.65	V
V_{IH}	Input High Voltage		3.0		V_{CC}+1	V
V_{OH1}	Output High Voltage	I_{OH} = −100 μA	3.7			V
V_{OH2}	Output High Voltage	I_{OH} = −1 mA	2.4			V
V_{OL}	Output Low Votlage	I_{OL} = 1.6 mA			0.45	V
P_D	Power Dissipation				800	mW

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

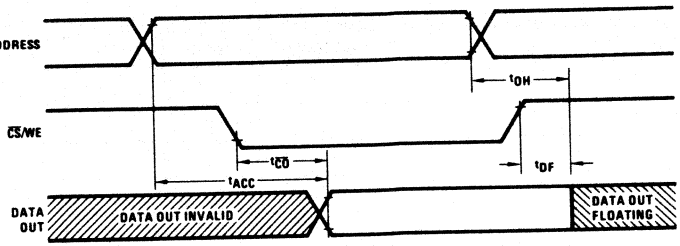
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ACC}	Address to Output Delay	Output Load: 1 TTL Gate and C_L = 100 pF		280	450	ns
t_{CO}	Chip Select to Output Delay	Input Rise and Fall Times ≤ 20 ns: Timing		60	120	ns
t_{DF}	Chip Deselect to Output Delay	Measurement Reference Levels: 0.8V	0		120	ns
t_{OH}	Address to Output Hold	and 2.8V for Inputs; 0.8V and 2.4V for Outputs, Input Pulse Levels: 0.65V to 3V	0			ns
CAPACITANCE, (Note 2)						
C_{IN}	Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1 MHz		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1 MHz

Note 3: Typical conditions are for operation at: T_A = 25°C, V_{CC} = 5V, V_{DD} = 12V, V_{BB} = −5V, and V_{SS} = 0V.

Switching Time Waveforms



Programming Instructions

Initially, and after each erasure, all bits of the MM2708 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CE}$/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O1–O8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to $N \times t_{PW} \geq 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Characteristics

$T_A = 25°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted

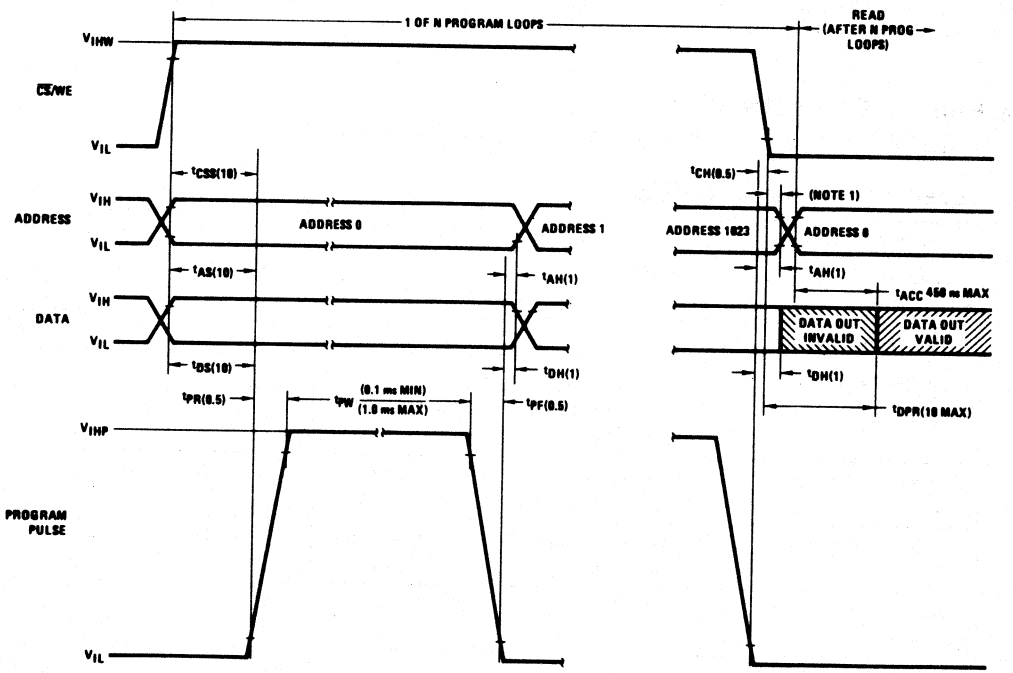
DC Programming Characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current	$V_{IN} = 5.25V$			10	μA
I_{IPL}	Program Pulse Source Current				3	mA
I_{IPH}	Program Pulse Sink Current				20	mA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, $T_A = 0°C$		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, $T_A = 0°C$		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, $T_A = 0°C$		34	45	mA
V_{IL}	Input Low Level (Except Program)		V_{SS}		0.65	V
V_{IH}	Input High Level, All Addresses and Data		3.0		$V_{CC}+1$	V
V_{IHW}	$\overline{CS}$/WE Input High Level	Referenced to V_{SS}	11.4		12.6	V
V_{IHP}	Program Pulse High Level	Referenced to V_{SS}	25		27	V
V_{ILP}	Program Pulse Low Level	$V_{IHP} - V_{ILP} = 25V$ Min	V_{SS}		1	V

AC Programming Characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AS}	Address Set-Up Time		10			µs
t_{CSS}	$\overline{CS}$/WE Set-Up Time		10			µs
t_{DS}	Data Set-Up Time		10			µs
t_{AH}	Address Hold Time		1			µs
t_{CH}	$\overline{CS}$/WE Hold Time		0.5			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Chip Deselect to Output Float Delay		0		120	µs
t_{DPR}	Program to Read Delay				10	µs
t_{PW}	Program Pulse Width		0.1		1.0	ms
t_{PR}	Program Pulse Rise Time		0.5		2.0	µs
t_{PF}	Program Pulse Fall Time		0.5		2.0	µs

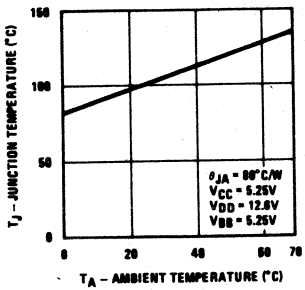
Programming Waveforms



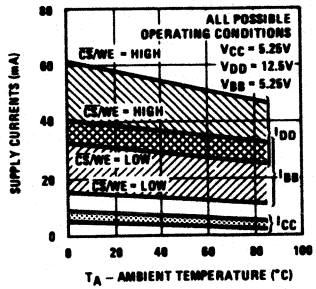
Note 1: The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.
Note 2: Numbers in parentheses indicate minimum timing in microseconds unless otherwise specified.

Typical DC Performance Characteristics

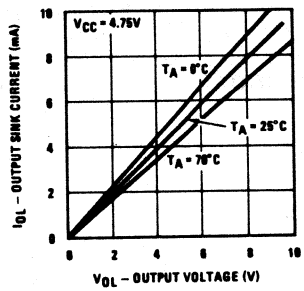
Maximum Junction Temperature vs Ambient Temperature



Range of Supply Currents vs Temperature

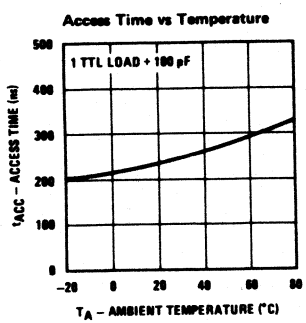

ALL POSSIBLE OPERATING CONDITIONS
V_{CC} = 5.25V
V_{DD} = 12.5V
V_{BB} = 5.25V
CS/WE = HIGH
CS/WE = HIGH
CS/WE = LOW
CS/WE = LOW
I_{DD}
I_{BB}
I_{CC}
SUPPLY CURRENTS (mA)
0
20
40
60
80
0
20
40
60
80
100
T_A – AMBIENT TEMPERATURE (°C)

Output Sink Current vs Output Voltage

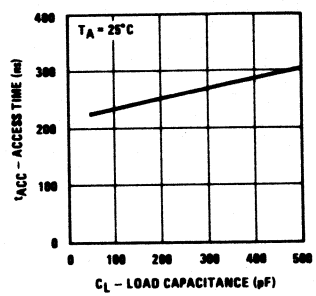


Typical AC Performance Characteristics

Access Time vs Temperature



Access Time vs Load Capacitance



2

National Semiconductor

MOS EPROMs

MM4203/MM5203 electrically programmable 2048-bit read only memory (pROM)

general description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

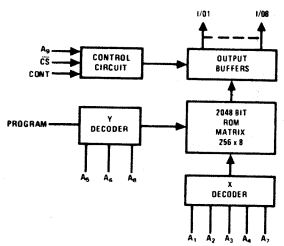
features

- Field programmable
- Bipolar compatibility — +5V, −12V operation
- High speed operation — 1μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

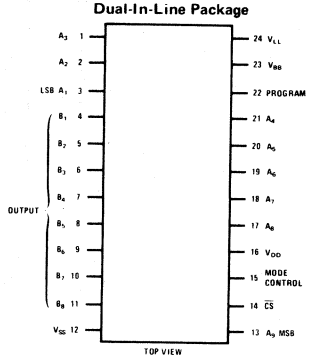
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams



Dual-In-Line Package

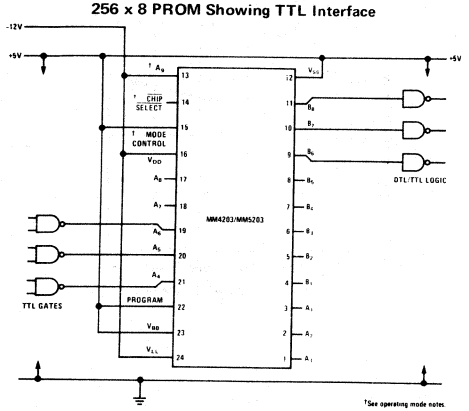


Order Number MM4203D or MM5203D
See Package 6

Order Number MM4203Q or MM5203Q
See Package 21

typical applications

256 x 8 PROM Showing TTL Interface



Note: For programming information see AN-100.

Operating Modes

256 x 8 ROM connection (shown)
Mode Control - HIGH (V_{SS})
Ag - LOW

512 x 4 ROM connections
Mode Control - LOW (GND or V_{DD})
Ag - Logic HIGH enables the odd (B_1, B_3, B_7) outputs
- Logic LOW enables the even (B_2, B_4 B_8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+.3V to −20V	Storage Temperature Range	−65°C to 125°C
Power Dissipation	1W	Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range MM4203	−55°C to 85°C		
MM5203	0°C to 70°C		

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{DD} = V_{LL} = −12V, ±5%, V_{BB} = PROGRAM = V_{SS} unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current, I_{LI}	V_{IN} = 0V			1	μA
Output Leakage, I_{LO}	V_{OUT} = 0V $\overline{CS}$ = V_{SS} - 2.0			1	μA
Power Supply Current, I_{SS}	T_A = 25°C $\overline{CS}$ = V_{SS} - 2.0		35	55	mA
Input LOW Voltage, V_{IL}		V_{SS} - 10		V_{SS} - 4.0	V
Input HIGH Voltage, V_{IH}		V_{SS} - 2.0		V_{SS} + .3	V
Output LOW Voltage, V_{OL}	1.6 mA sink −12.6V < V_{LL} < −3V			.40	V
Output Clamp Current, I_{CF}	V_{LL} = -3.0V V_{OUT} = -1.0V (Note 8) T_A = 0°C		3.5	6.0	mA
	V_{LL} = -12.6V V_{OUT} = -1.0V (Note 8) T_A = 0°C		8.0	15.0	mA
Output HIGH Voltage, V_{OH}	0.8 mA source	2.4			V
Data Hold Time, T_{OH}	(Min Access Time) Figures 1 & 2			100	ns
Access Time, T_{ACC}	T_A = 25°C Figures 1 & 2 (Note 6)		.700	1	μs
Chip Select Time, T_{CO}	Figures 1 & 3			500	ns
Chip Deselect Time, T_{OD}	Figures 1 & 3			500	ns
Allowable Chip Select Delay, t_{CS}	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
Input Capacitance, C_{IN}	V_{IN} = V_{SS} } f = 1.0 MHz (Note 2)		8	15	pF
Output Capacitance, C_{OUT}	V_{OUT} = V_{SS} } $\overline{CS}$ = V_{SS} - 2.0		8	15	pF

programming characteristics (see Figure 4)

T_A = 25°C, V_{SS} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current, I_{LD}	V_{IN} = −50V		0	10	mA
Program Load Current, I_{LP}	V_{IN} = −50V		0	10	mA
V_{BB} Supply Load Current, I_{LB}			0	10	mA
Peak I_{DD} Supply Load Current I_{LDD} (Note 3)	V_{DD} = $V_{program}$ = −50V		650		mA
Input High Voltage, V_{IHP}		−2		+.3	V
Address and Data Input Low Voltage, V_{ILP}		−50		−40	V
Pulsed Input Low Voltage:					
V_{DD}, and Program, V_{DLP}		−50		−48	V
V_{LL}	(Note 5)	−50		0	V
V_{DD} Pulse Duty Cycle				2	%
Program Pulse Width, t_{PW} (Note 4)	V_{DD} = $V_{program}$ = −50V			20	ms
Data and Address Set Up Time, t_{DW}		1			μs
Data and Address Hold Time, t_{DH}		0			μs
Pulsed V_{DD} Supply Overlap, t_{SS}		1		100	μs
Pulsed V_{DD} Supply Overlap, t_{SH}		−.1		3	ms
V_{DD}, Program, Address, and Input Rise and Fall Times				1	μs

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of A9 and MODE CONTROL.

Note 2: Capacitances are not tested on a production basis but are periodically sampled.

Note 3: I_{DDP} flows only during program period t_{PWP}. Average power supply current I_{LDD} is typically 15 mA at 2% duty cycle.

Note 4: Maximum duty cycle of t_{PW} should not be greater than 2% of cycle time so that power dissipation is minimized. The program cycle should be repeated until the data reads true, then over-program three times that number of cycles (symbolized as X+3X programming.

Note 5: V_{LL} is not needed during programming but may be tied to V_{DD} for convenience.

Note 6: T_{ACC} = 1000 ns + 25(N-1) where N is the number of chips wired-OR together.

Note 7: Measured under continuous operation.

Note 8: I_{CF} flows out the V_{LL} pin, it does not flow out the V_{DD} pin.

access time diagrams

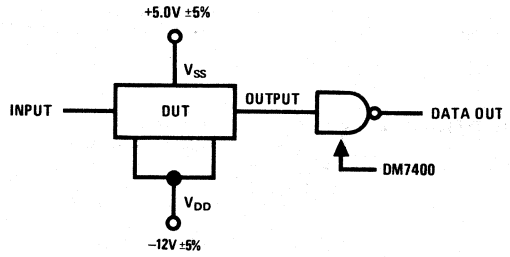


Figure 1

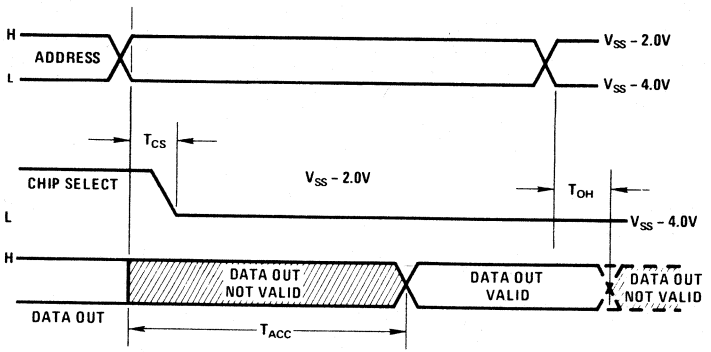


Figure 2

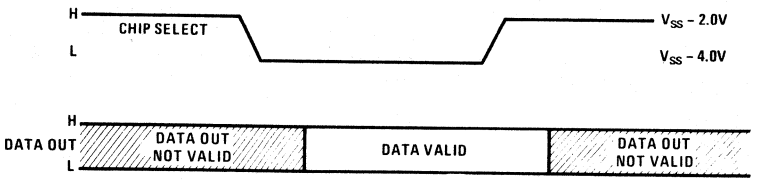


Figure 3

program waveforms

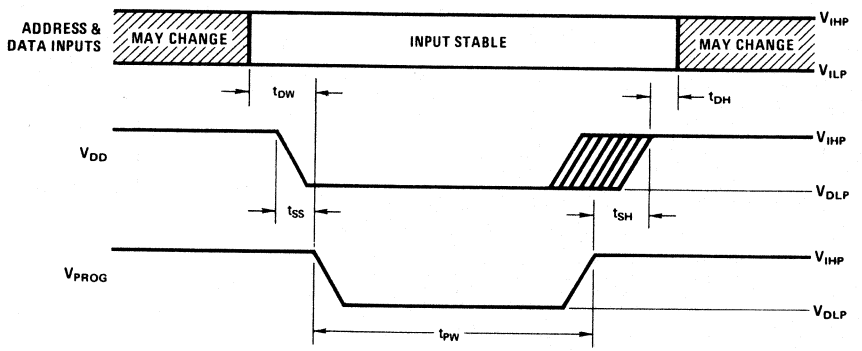


Figure 4

operation of the MM4203/MM5203 in program mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. (Note 1)

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. The address should be applied for at least 1 μs before application of the Program pulse. In programming mode, data inputs 1–8 are pins 4–11 respectively regardless of the logic state of A_9 and mode control. Chip select should be disabled (HIGH).

Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

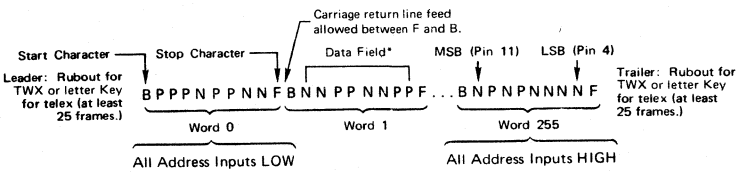
MODE	DATA AND ADDRESS LINES		V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
	HIGH	LOW						
Read	V_{SS} −2.0	V_{SS} −4.0	+5	V_{SS}	−12	V_{SS}	V_{SS} − 4V	−3V to −12V
Program	V_{SS} −2.0	V_{SS} − 40	GND	+12	−48 (Pulse)	−48 (Pulse)	GND	GND to −50V

erasing procedure

The MM4203Q/MM5203Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-2 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4203/MM5203 should be placed about one inch away from the lamp for about 20—30 minutes.

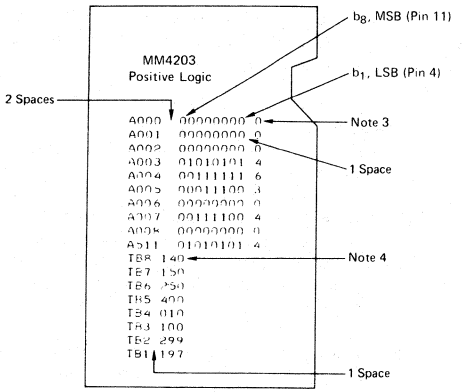
preferred tape format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

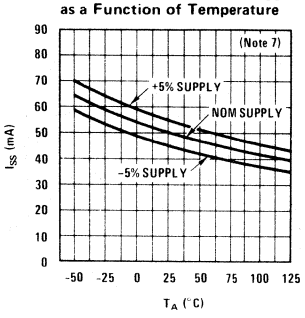
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

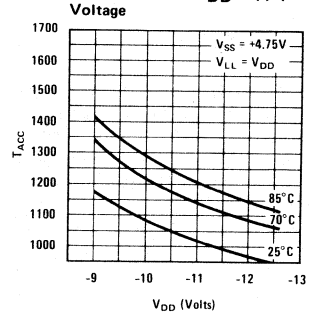
Note 4: The total number of "1" bits in each output column or bit position.

typical performance characteristics

Maximum Supply Current I_{SS} as a Function of Temperature



Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage



National Semiconductor

MOS EPROMs

MM4204/MM5204
electrically programmable 4096-bit read only memory (EPROM)

general description

The MM4204/MM5204 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatiblity. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

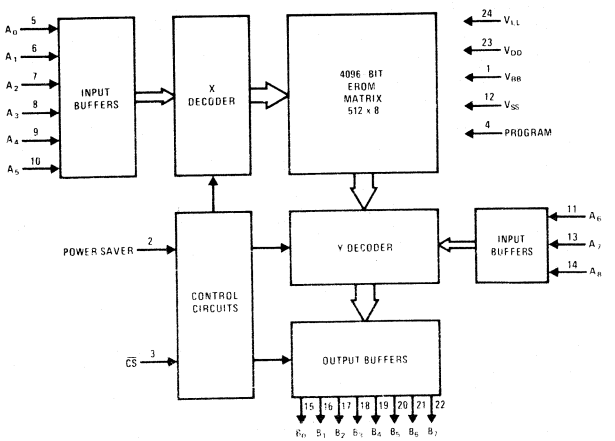
features

- Field programmable
- Fast program time: ten seconds typical for 4096-bits
- Fast access time
  - MM4204 1.25μs
  - MM5204 1μs
- DTL/TTL compatibility
- Standard power supplies 5.0V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications

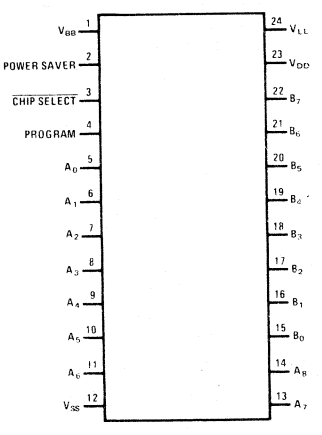
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

block and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4204D
or MM5204D
See Package 6

Order Number MM4204Q
or MM5204Q
See Package 21

2

absolute maximum ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204	0°C to +70°C
MM4204	−55°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10.0	mA
I_{SS}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

ac electrical characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C, *(Figure 1)*, (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, *(Figure 1)*, (Note 4)			1.25	μs
t_{PO}	Power Saver Set-Up Time					
	MM5204	*(Figure 1)*			1.8	μs
	MM4204	*(Figure 1)*			2.0	μs
t_{CO}	Chip Select Delay					
	MM5204	*(Figure 1)*			500	ns
	MM4204	*(Figure 1)*			600	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
t_{ODP}	Power Saver Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

programmer electrical characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, (see *Figure 2*), (Note 5).

	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address Input Low Voltage		50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHP}	V_{DD} and Program High Voltage		2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_R, t_F	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 1000 ns + 25 (N-1) where N is the number of devices wire−OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EROM is initially programmed with all "0's." A V_{IHP} on any data input B0−B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0−B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and $T_A = 25°C$, unless otherwise specified.

erase specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm^2.

programming

The MM4204/MM5204 is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0−A8. Data inputs are B0−B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B0−B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0−B7 will write a logic "1" into that location.

programming (cont.)

National offers programmer options with both the IMP16-P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16-P	IMP-16P/805
IPC-16P	IPC-16P/805

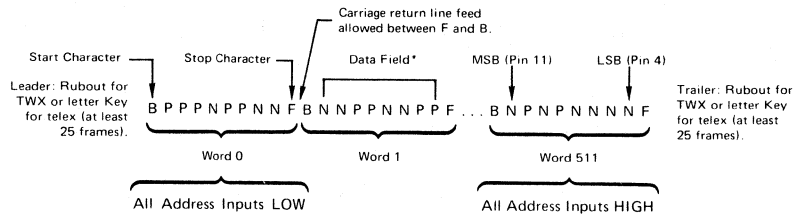
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

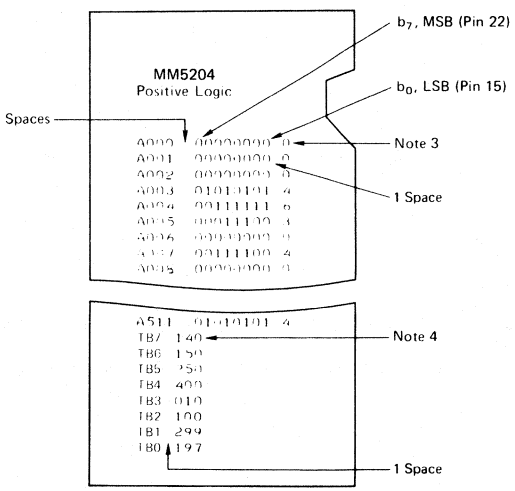
preferred format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

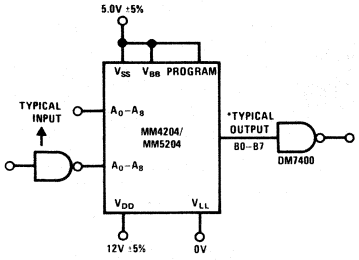
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

erasing procedure

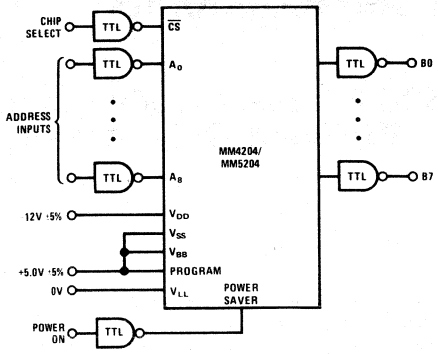
The MM4204Q/MM5204Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worse case time required with the equipment. Then over-erase by a factor of 2,i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4204/MM5204 should be placed about one inch away from the lamp for about 20—30 minutes.

ac test circuit

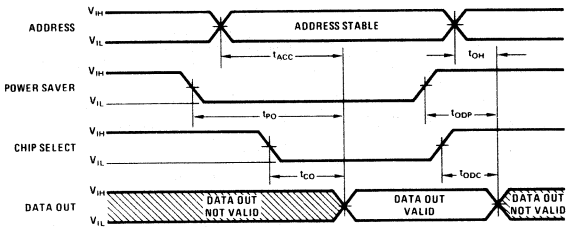


*t_{ACC}, t_{OH}, t_{CO}, and t_{OD} measured at output of MM4204/MM5204.

typical application



switching time waveforms



Note: All times measured with respect to 1.5V level with t_R and t_F ≤ 20 ns.

FIGURE 1. Read Operation

programming waveforms

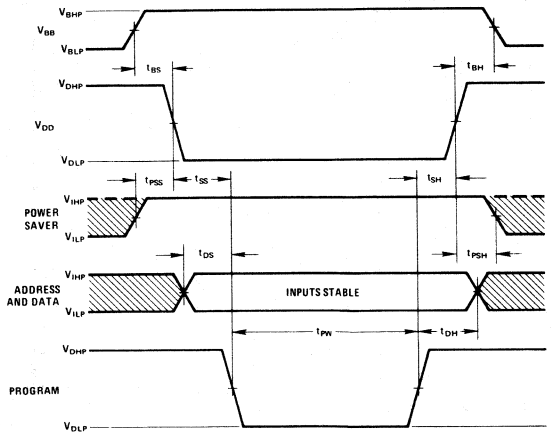


FIGURE 2. Programming Waveforms

National Semiconductor

DECEMBER 1977

MM5204-1 Electrically Programmable 4096-Bit Read Only Memory (EPROM)

General Description

The MM5204-1 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver", is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications
- Compatible with SC/MP II N-channel microprocessor

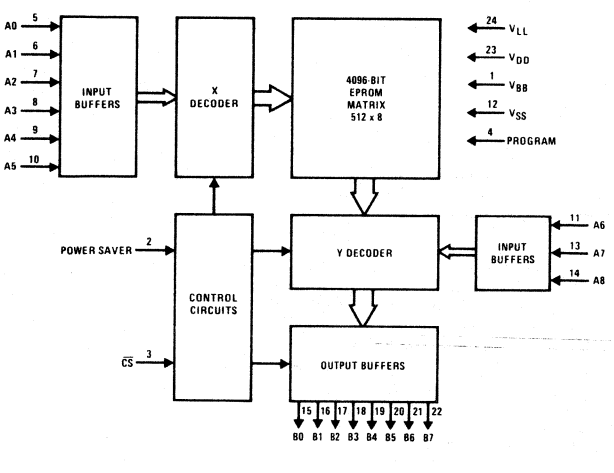
Features

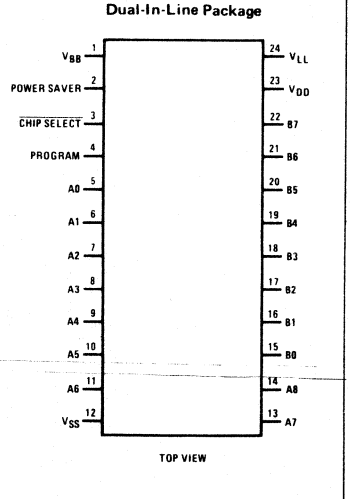
- Field programmable
- Fast program time: ten seconds typical for 4096 bits
- Fast access time
  MM5204-1 700 ns
- DTL/TTL compatibility
- Standard power supplies 5V, −12V

Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

Block and Connection Diagrams





IM-B20M127/Printed in U.S.A.

Absolute Maximum Ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Operating Temperature Range	
MM5204-1	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS} 14		V_{SS} 4.2	V
V_{IH}	Input High Voltage		V_{SS} 1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		V_{LL}	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	T_A = 0°C, $\overline{CS}$ = V_{IH},				
		Power Saver = V_{IL}		28	40.0	mA
		Power Saver = V_{IH}		6.0	8.0	mA
I_{SS}	V_{SS} Current	T_A = 0°C, CS = V_{IH}				
		Power Saver = V_{IL}			42	mA
		Power Saver = V_{IH}			10	mA

AC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time	T_A = 70°C, *(Figure 1)*, (Note 4)			700	ns
t_{PO}	Power Saver Set-Up Time	*(Figure 1)*			1.4	μs
t_{CO}	Chip Select Delay	*(Figure 1)*			250	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time	*(Figure 1)*	30	200	500	ns
t_{ODP}	Power Saver Deselect Time	*(Figure 1)*	30	200	500	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

Programmer Electrical Characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, *(Figure 2)*, (Note 5).

PARAMETER		CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = 18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = 50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		2.0		0.3	V
V_{ILP}	Address Input Low Voltage		50		11	V
	Data Input Low Voltage		18		11	V
V_{DHP}	V_{DD} and Program High Voltage		2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		50		48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_r, t_f	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 700 ns + 25 (N-1) where N is the number of devices wire−OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EPROM is initially programmed with all "0's." A V_{IHP} on any data input B0−B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0−B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and $T_A = 25°C$, unless otherwise specified.

Erase Specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm².

Programming

The MM5204-1 is normally shipped in the unprogrammed state. All 4096 bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0−A8. Data inputs are B0−B7 and write operation is controlled by pulsing the Program input. Since the EPROM is initially shipped with all "0's", a V_{IHP} on any data input B0−B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0−B7 will write a logic "1" into that location.

Programming (Continued)

National offers a programming option with the SC/MP Low Cost Development System (LCDS).

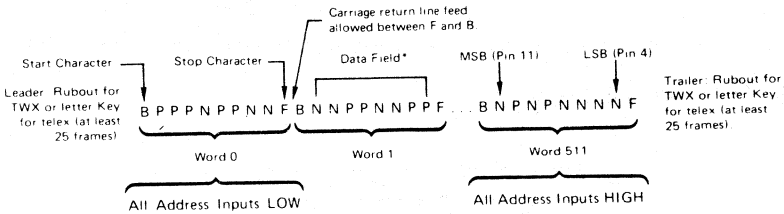
See application note AN-189 for a description, or contact the local sales office for further information. There are also several commercial programmers available.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

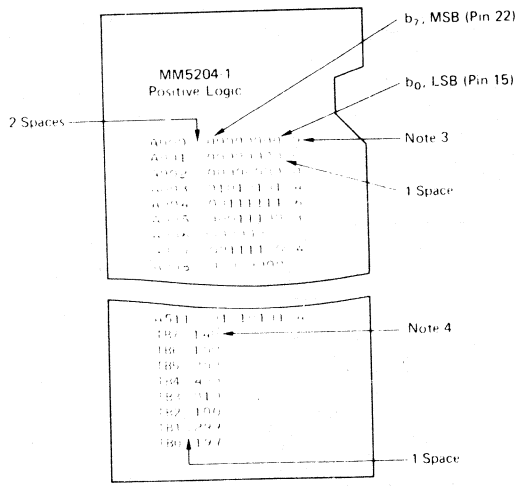
Preferred Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

Alternate Format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

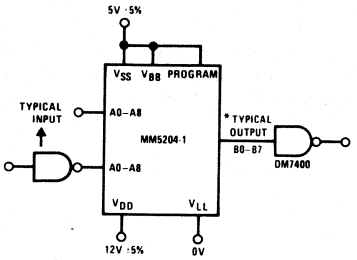
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

Erasing Procedure

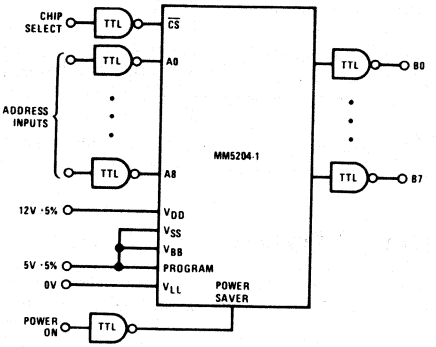
The MM5204-1 may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM5204-1 should be placed about one inch away from the lamp for about 20—30 minutes.

AC Test Circuit

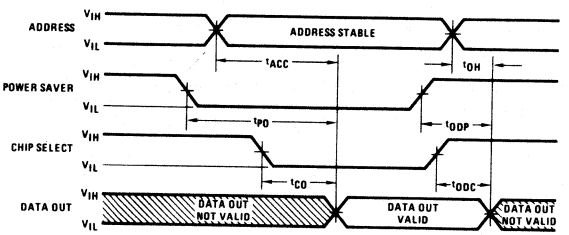


*t_{ACC}, t_{OH}, t_{CD} and t_{OD} measured at output of MM5204-1

Typical Application



Switching Time Waveforms



Note. All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns

FIGURE 1. Read Operation

Programming Waveforms

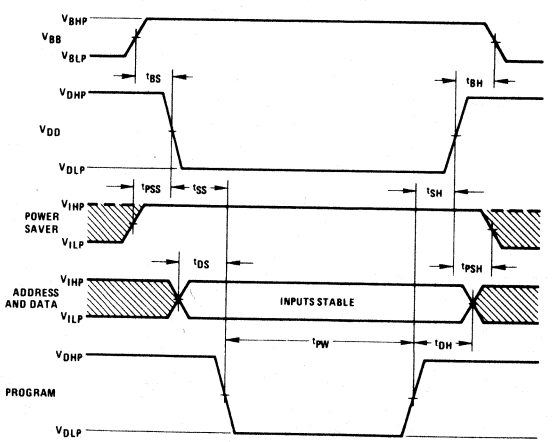


FIGURE 2. Programming Waveforms

INTRODUCTION

This technical guide describes National's family of semiconductor EPROMs – erasable programmable read only memories. It is written to help the digital system designer select and apply National EPROMs to yield the most efficient systems possible.

Three National EPROMs are described:

M1702A, a 2K memory and direct replacement for the Intel 1702A.

MM5203, a 2K memory.

MM5204, a 4K memory.

CONTENTS

SECTION I
INTRODUCTION TO NATIONAL EPROMS

Each major step in the evolution of read only memories (ROMs) has given the user more flexibilty and choice in designing digital systems. Early advances in ROM technology made fixed-program storage more economical and gave the designer more latitude in memory size and organization. They also made possible memories of smaller dimensions.

Programmable ROMs (PROMs) went a step further by enabling the designer to dictate the pattern of the programmed data, which the memory is to store, entered in the device either at the factory before shipment or by the user after shipment.

Erasable PROMs (EPROMs) represent the next logical step. National EPROMs put erase and reprogram capabilities into the designer's hands. Using EPROMs, the designer is free to make changes, and can create the best possible system for the particular purpose because EPROMs can be erased and reprogrammed as often as needed to accommodate those changes, up to the time of final design, if neccessary.

EPROMs permit design flexibility increased bit density, low inventory cost, and easy system assembly and test. But they must be programmed, erased, and used in the system correctly if they are to provide these benefits in addition to low reject rates and high field reliability.

1. General advantages to the designer.

Besides the ability to program, erase, and reprogram as many times as desired, the user of National EPROMs can also take advantage of these other features:

- MOS silicon-gate technology, which permits bipolar compatibility, higher-performance MOS circuits, and higher functional density per chip than conventional MOS technologies.
- Fast programming and access
- Design flexibility, with bipolar, DTL and TTL compatibility, simple memory expansion, and pin compatibility with National's mask-programmable ROMs.
- Input protection against static charge.
- Non-volatile storage. (National's tests indicate data retention for at least 20 years under proper conditions.)
- Quick turnaround from order to shipment.

The most distinguishing feature of the EPROM is the erasability of data by ultraviolet light. That process is understood more quickly and easily if we first view the basic EPROM storage cell and how the cell is programmed.

2. The FAMOS storage cell.

The basic EPROM cell is a Floating-gate, Avalanche-injection, MOS (FAMOS) field-effect transistor. It is a P-channel device with a floating polysilicon gate. The gate is insulated from the silicon substrate by an SiO_2 layer of ~ 1000 Å and from the top surface by ~ 1 μm of vapox-deposited oxide.

There is no electrical access to the gate electrode; thus no electrical contact is made with the gate. (See Figure 1.)

- **How it is programmed.**

To program the cell, a charge of electrons must reach the floating gate. This is achieved by applying a junction voltage of greater than -30 volts to the P-channel drain which in turn causes an injection of high-energy electrons from the avalanche region of the device, through the 1000 Å $Si0_2$ layer and onto the floating gate.

The charge of electrons accumulates on the floating gate and stays there even after the junction voltage is discontinued. The charge (program data) is thus stored, since the eletrical field is not strong enough to transport the electrons over the "wall" formed by the floating gate's thermal-oxide insulation. (See Figure 34, Appendix.)

After 10 years, 70 percent of the originai charge will still be present in the cell if the operating temperature has been limited to 125°C. This was determined by plotting diminishing charge (charge decay) as a function of time at 125°C and 300°C, and extrapolating the 300°C data.

- **How it is erased.**

Removing the charge (erasing the data) requires energy of a form other than electrical, because the charges stored at the floating gate cannot be accessed electrically.

Therefore the FAMOS cell is exposed to ultraviolet light of the proper intensity and wavelength. This photon energy (or photocurrent) excites the stored electrons "over the wall" of thermal-oxide insulation, away from the floating gate, back to the avalanche region where it orginated, and finally to the drain.

The floating gate is thus discharged; the FAMOS cell is empty of data and ready to be reprogrammed. (See Figure 35, Appendix.)

- **Erase procedure for the user.**

Each National EPROM designated "Q"is packaged with a transparent quartz lid. Through the lid, the user may expose the device to ultraviolent light in order to erase the bit pattern. The procedure includes these steps:

1.) Use a source (lamp) that emits high-intensity, short-wave, ultraviolet light. Examples of lamps that can erase a bit pattern in 10 to 20 minutes are listed in Table M (Appendix); National has evaluated and approved these for use with the company's EPROMs.
2.) Place the memory to be erased about one inch from the lamp tubes. Do not use short-wave filters.
3.) Expose the memory to light at a wavelength of 2537Å. The recommended integrated dose (UV intensity x exposure time) is 6W-sec/cm^2.

Since there is no absolute rule regarding erase time, establish the worst-case exposure time required by the equipment. Then over-erase exposure by a factor of 2. For example, if the device appears to erased after 8 minutes of exposure, continue the exposure for an additional 16 minutes for a total of 24 minutes. This over-erasing may be expressed as x + 2x.

Calibrate the UV lamp monthly, since UV output varies during the lifetime of the lamp.

3. Program/erase considerations: key to EPROM performance.

The programming and erasing of EPROMs are so strongly interrelated that this primary rule is to be followed:

In the event of any programming problem, first check the erase function. In the event of any erase problem, first check the programming function.

For best results in programming EPROMs, National recommends that designers not build their own programmers but use, instead, any of the commercially available programmers listed in Table L (Appendix) which have been approved by National for use with the company's EPROMs.

Figure 1. FAMOS storage cell of a National Eprom.

Cross section of the cell at equilibrium (zero charge). The presence or absence of charge in the FAMOS cell can easily be detected at any time by measuring the conductance between the source and the drain.

Figure 2. Floating-gate programming characteristics.

This diagram, which plots floating-gate charge vs. programming time, is applicable to all National EPROMs; only the value of "A" varies: for the

MM1702, A = 4; for the

MM5203, A = 3; and for the

MM5204, A = 5. In all cases, x min = 1 ms and x max = 200 ms.

Figure 3. Floating-gate erase characteristics.

This diagram, which plots floating-gate charge vs erase time, illustrates the over-erasing method (x + 2x) discussed in the text. National's erase procedure is based on a recalibration of the erase system every three months and calibration for three time-constants.

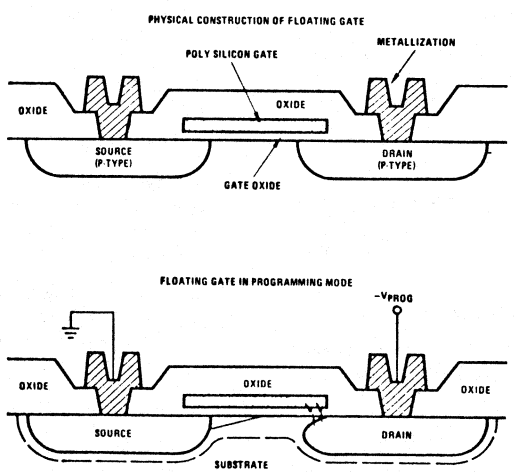


FIGURE 1. FAMOS Storage Cell

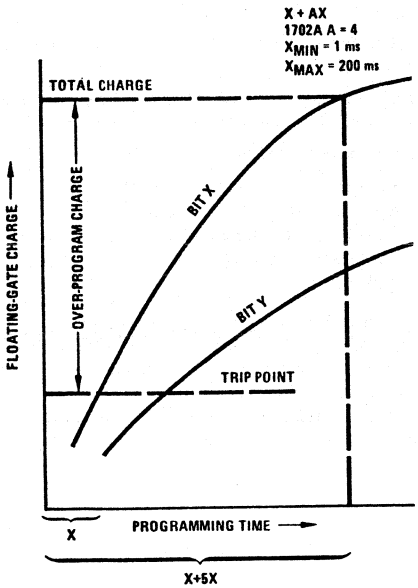


FIGURE 2. Floating-Gate Characteristics Interactive Programming

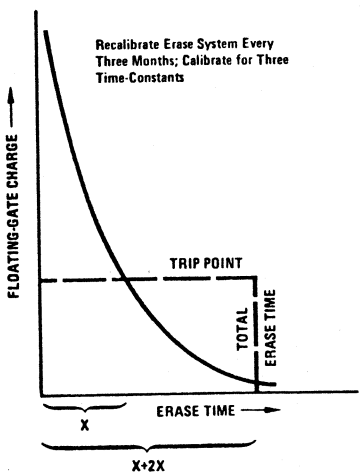


FIGURE 3. Floating-Gate Erase Characteristic

Figure 4. UV Intensity (In Voltage) as a Function of Time (In seconds).

The UV output to photon energy of 4.9#eV (2537 Å), while the built-in field surrounded by oxide is 4.3#eV. Because the photon energy is greater, it moves the electrons and transports the charge from the floating gate.

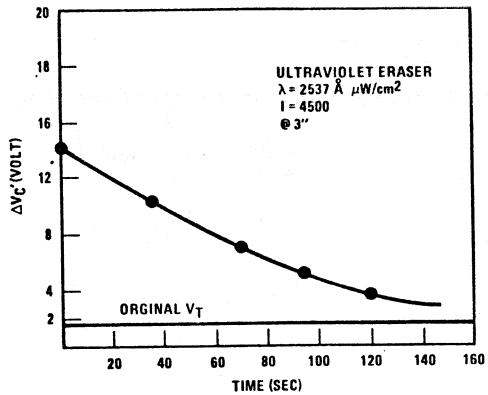


FIGURE 4. UV Intensity Vs. Time

When programming, the user must be alert to many and varied considerations such as those that follow:

- Out-of-specification voltages – usually in the programming mode and detectable with an oscilloscope
- Older instruments – may need modifications such as filters to eliminate transients
- Socket performance – sockets are expensive, and even a replacement may malfunction. Since most programmers do not have continuity-test features, socketing problems usually appear to be device-oriented
- Wide swings in voltage – be sure driver circuits cover these contingencies
- Timing – critical, and must be correctly maintained
- A satisfactory program algorithm – fixed time vs. interactive . . . – must be determined before programming
- The effect of heat on programming performance – see figures of temperature-sensing circuits in Appendix

Calibrate the programmer weekly, and always refer to the data sheet or technical description accompanying the instrument.

Calibrate the erase system monthly. The recommended procedure for such calibration is found in Table N (Appendix). This procedure is applicable to all erase systems listed in Table M.

4. Basic similarities.

The three EPROMs described here are erasable, electrically programmable, MOS read-only memories with the following features in common:

- Silicon gate technology – for higher-performance MOS circuits and higher functional density on a monolithic chip.
- Static MOS circuitry – no clocks required
- TRI-STATE output – Or-tie capability and common data busing
- Non-volatile storage – data retention despite power interruptions
- Fast programming and access – exact figures differ among the EPROMs and are provided in Section III
- Compatilibity – Bipolar, DTL, TTL; pin-compatibility with National mask programmable ROMs
- 24-pin dual-in-line organization
- Simple memory expansion – chip-select input pin and output control
- Guaranteed all-bit programmability – 100-percent factory testing; all bits are also fully decoded
- Standard power supplies
- Common applications of the EPROMs include code conversion, random logic synthesis, pattern experimentation, table look-up, character generation, microprogramming and, with the MM5204, electronic keyboards.
- Each of the EPROMs will drive MOS circuitry. All can be shipped unprogrammed. All may be programmed by use of a -50 volt pulse to store a charge in a cell location, as explained in Section I. Further programming details are explained in the individual EPROM descriptions in Section III.

SECTION II
THE MM1702AQ, MM5203P, AND MM5204Q

1. The MM1702A EPROM

The National MM1702A is a 256-word by 8-bit ROM that is electrically programmable and is erasable by ultraviolet light. It is a direct replacement for the Intel 1702A and is ideally suited to uses where fast turn-around and pattern experimentation are important.

The MM1702A may be used to design prototype or initial-run systems, which then can be produced in large volume using the even more economical MM1302, a pin-for-pin compatible mask-programmed National ROM.

The following figures illustrate the structure, operating chatacteristics and programming chatacteristics of the National MM1702A.

Structure

Figure 5. Logic and Pin Configuration.

Logic Symbol.

Pin Assignment.

Pin Names.

Figure 6 Block Diagram.

Operating Characteristics

Figure 7. Typical Performance Characteristics.

Table A. Electrical Characteristics . . dc.

Table B. Capacitance Characteristics.

Figure 8. Input Characteristics.

a. Input buffer. (Input protection.)

b. Input levels. High and low voltage (logic) levels. They are TTL-compatible and will function with normal MOS levels.

Figure 9. Output Characteristics.

a. Output buffer. This circuit diagram indicates how the chip select control (with Tri-State output) turns off both transistors and places the buffer in a high-impedance state.

b. Output levels. Like the input levels, they are TTL-compatible and will function with normal MOS levels.

Table C. Electrical Characteristics . . ac.

Figure 10. Read Operation Timing.

Figure 11. Power-Down Timing.

Programming Characteristics

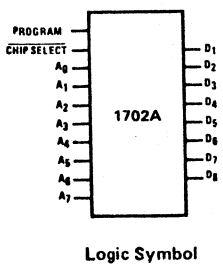
Figure 12. Program Waveforms.

Table D. Program Operation Characteristics.

a. dc.

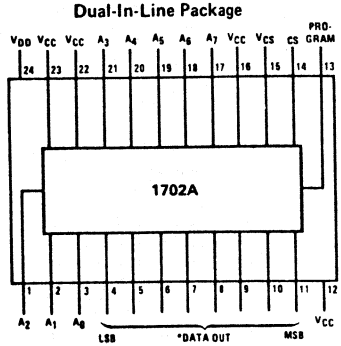
b. ac.

Table E. Read/Program Voltage.



Logic Symbol

Dual-In-Line Package



Top View

Pin Assignment

*The pin in the data input lead during programming

PIN NAMES

A_0-A_7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{out\,1}$-$D_{out\,8}$	Data Outputs

FIGURE 5. Logic and Pin Configuration – 1702A

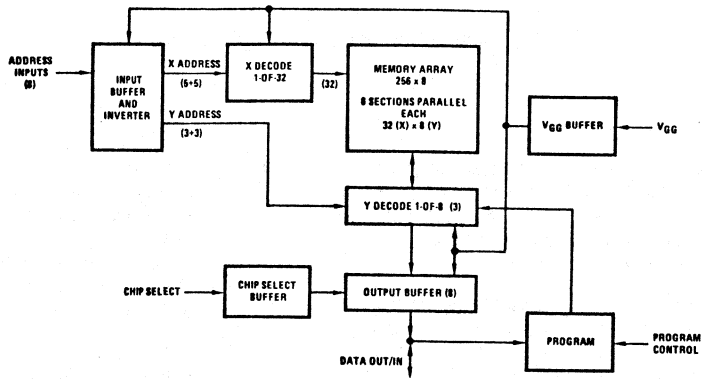


FIGURE 6. Block Diagram – 1702A

typical performance characteristics

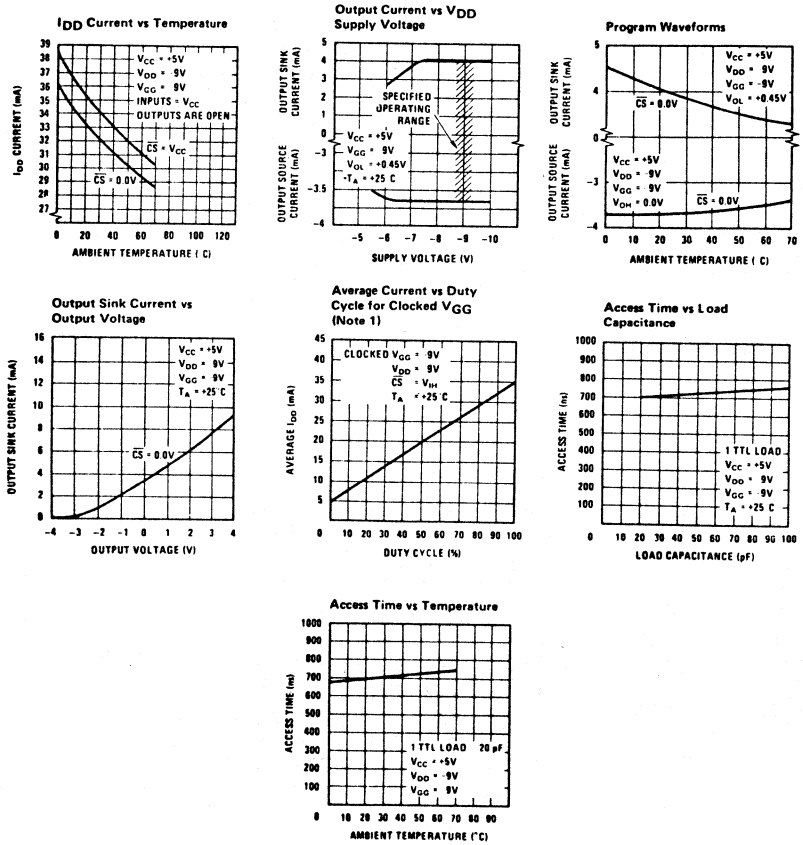


FIGURE 7. Typical Performance Characteristics – 1702A

read operation dc characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0.0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2			1	μA
I_{DDO}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} −2 I_{OL} = 0.0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1.0, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1.0		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{OL}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{OH}	Output Source Current	V_{OUT} = 0.0V	−2.0			mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{OH}	Output High Voltage	I_{OH} = 100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option. V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DD0} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1702AL.

TABLE B – 1702A

capacitance characteristics $T_A = 25°C$ (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused $V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are $\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance (Note 1)	At ac Ground $V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

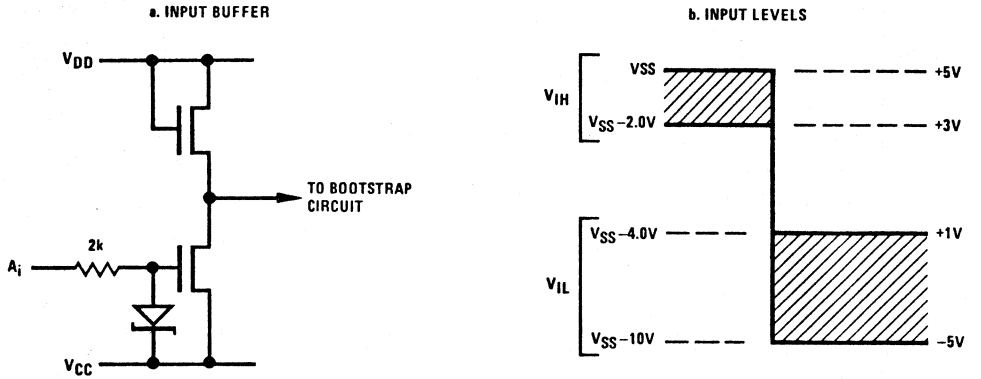


FIGURE 8. Input Characteristics – 1702A

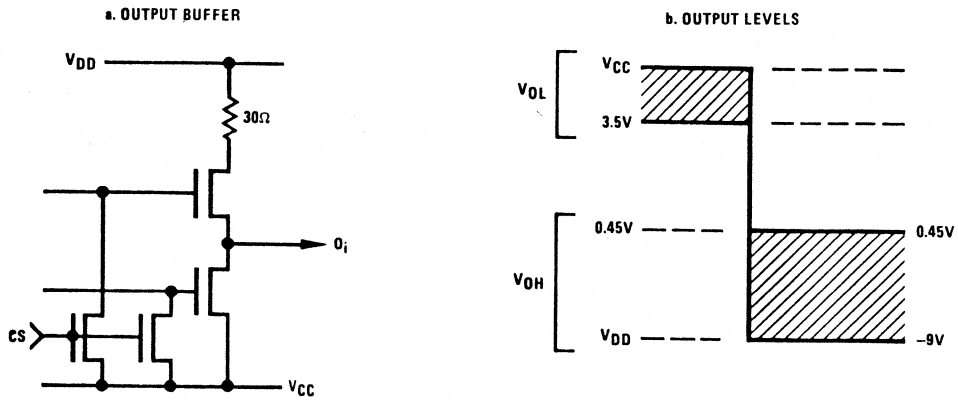


FIGURE 9. Output Characteristics – 1702A

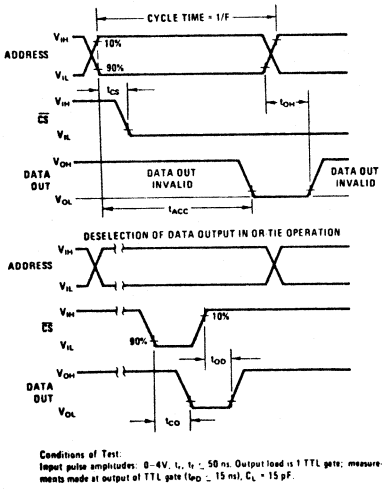
TABLE C. Electrical Characteristics —AC — 1702A

read operation ac characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	µs
t_{DVGG}	Clocked V_{GG} Set-Up (Note 2)	1			µs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{OD}	Output Deselect			300	ns
t_{OHC}	Data Out Hold in Clocked V_{GG} Mode (Note 1)			5	µs

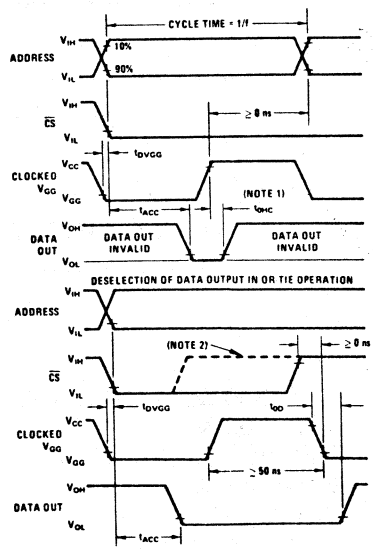
(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq$ 50 ns. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq$ 15 ns), C_L = 15 pF.

FIGURE 10. Read Operation Timing — 1702A

(b) Power-Down Option (Note 1)

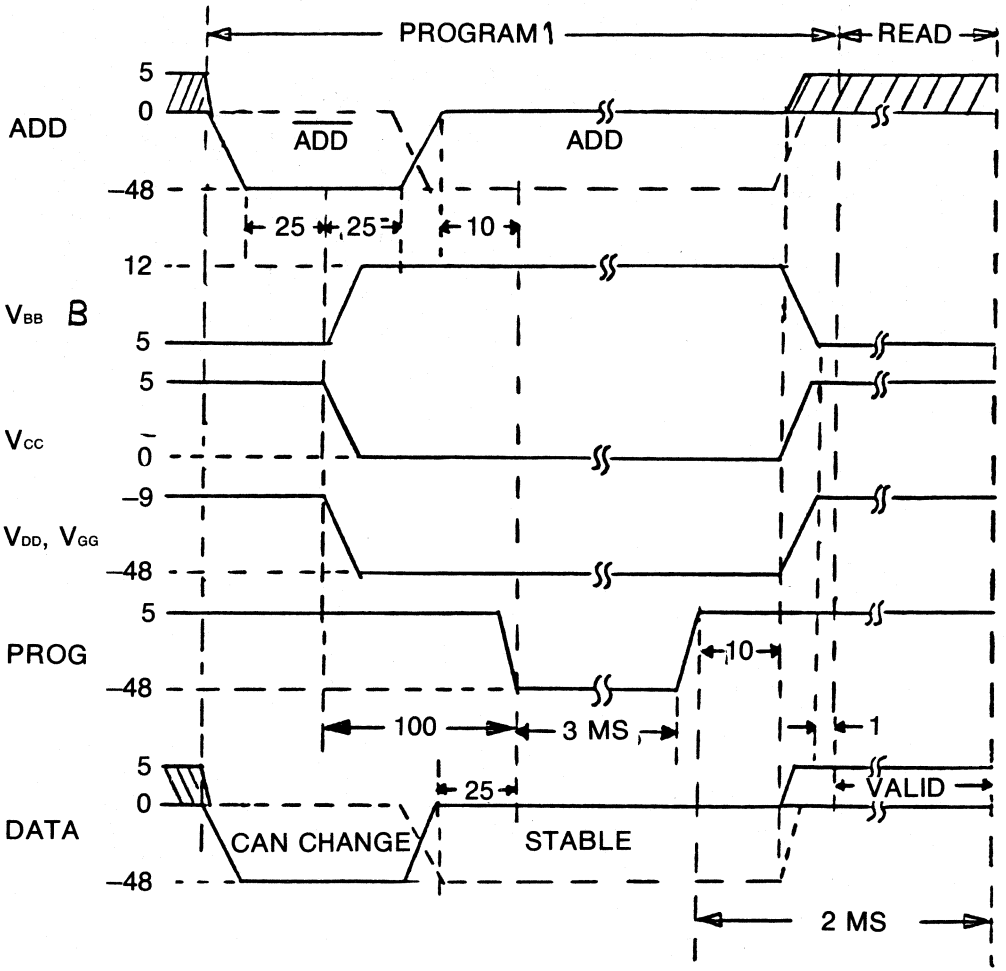


Note 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown on static operation with constant V_{GG}.

FIGURE 11. Power-Down Timing — 1702A

2



$I_{DD} > 300$ MA FOR NO MORE THAN 100 US
$I_{BB} \leqq 100$ MA
20% MAX DUTY CYCLE
RISE, FALL $\leqq$ 1 US
"O" STATE
8 BITS AT ONCE
X+4X (TYP 30 SEC)

FIG 12 PROGRAM-1702A

TABLE D. Programming Characteristics — 1702A

a. dc. programming operation dc characteristics

T_A = 25°C, V_{CC} = 0V, V_{BB} = 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI1P}	Address and Data Input Load Current	V_{IN} = −48V			10	mA
I_{LI2P}	Program and V_{GG} Load Current	V_{IN} = −48V			10	mA
I_{BB}	V_{BB} Supply Load Current	(Note 5)		10	100	mA
I_{DDP}	Peak I_{DD} Supply Load Current	V_{DD} = V_{PROG} = −48V V_{GG} = 35V (Note 4)		200	300	mA
V_{IHP}	Input High Voltage				0 3	V
V_{IL1P}	Pulsed Data Input Low Voltage		46		48	V
V_{IL2P}	Address Input Low Voltage		40		48	V
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage		46		48	V
V_{IL4P}	Pulsed Input Low V_{GG} Voltage		35		40	V

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100μs. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100 mA max. current to prevent damage to the device.

b. ac. programming operation ac characteristics

T_A = 25°C, V_{CC} = 0V, V_{BB} = 12V ±10%, $\overline{CS}$ = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle (V_{DD}, V_{GG})				20	%
t_{OPW}	Program Pulse Width	V_{GG} = 35V, V_{DD} V_{PROG} = 48V			3	ms
t_{DW}	Data Set-Up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{DD}, V_{GG} Set-Up		100			μs
t_{VD}	V_{DD}, V_{GG} Hold		10		100	μs
t_{ACW}	Address Complement Set-Up	(Note 6)	25			μs
t_{ACH}	Address Complement Hold	(Note 6)	25			μs
t_{ATW}	Address True Set-Up		10			μs
t_{ATH}	Address True Hold		10			μs

Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0–255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by x + 4x.)

Programming the MM1702A

All 2048 bits of the MM1702A are in the "0" state (output low). Information is introduced by selectively programming "1"s (output high) in the proper bit locations.

Word addresses are selected by the same decoding circuitry used in the Read mode. When the pulsed V_{DD} and V_{GG} move to their negative levels, all eight address bits must be in the binary complement state, and the addresses must be held there for at least 25 μs after V_{DD} and V_{GG} have moved. The addresses must then make the transition to their true state at least 10 μs before the program pulse is applied.

Program the addresses in the sequence 0-255 at least 32 times. Use the eight output terminals as data inputs to determine the information pattern in the eight bits of each word. A low data input level (-48V) will program a "1"; a high data input level (ground) will leave a "O" (See Table E).

Setting the desired bit information patterns on the data input terminals programs all eight bits of a word simultaneously.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

TABLE E. Read/Program Voltages — 1702A

	READ		PROGRAM		
PIN	HI	LO	HI	LO	MAX I
ADD	$V_{CC}-2$ to V_{CC}	V_{DD} to $V_{CC}-4.1$	0	−40 to −48	10mA
DATA (Outputs)	3.5 to V_{CC}	V_{DD} to 0.45	0	−46 to −48	10mA
CS	$V_{CC}-2$ to V_{CC}	V_{DD} to $V_{CC}-4.1$	0	–	–
PROG	5	–	0	−46 to −48	–
P22, P23 V_{CC}	5	–	0	–	–
V_{BB}	5	–	12	–	100mA
V_{DD}	−9	–	0	−46 to −48	300mA
V_{GG}	−9	–	0	−35 to −40	10mA

2) The MM5203 EPROM
(Military MM4203)

The National MM5203 is a 2048-bit ROM that is electrically programmable and is erasable by ultraviolet light. The programmable memory is organized as 256 words of 8-bits each or organized as 512 by 4 bits. 5203 is electrically selectable between the two modes.

The MM5203 is pin-compatible with National's MM5213 and MM5231 mask-programmable ROMs.

The following figures and tables illustrate the structure, operating characteristics, and programming characteristics of the National MM5203.

Structure

Figure 13. Logic and Pin Configuration.
Logic symbol.
Pin Assignment.
Pin Names.

Figure 14. Block Diagram.

Operating Characteristics

Figure 15. a. Typical performance characteristics.
b. Access time vs V_{DD} and temperature.

Figure 16. Input Characteristics.
a. Input buffer.
b. Input levels.

Figure 17. Output Characteristics
a. Output buffer. Note that in the case of the MM5203, the V_{LL} provides independent control on the output V_{OL}.
b. Output levels.

Figure 18. Read Operation Timing.

Table G. Read Conditions.

Figure 19. Program waveforms.

Table H. Program Conditions.

Figure 20. Output structure, unique to MM5203. V_{LL} is used for output V_{OL} only , and can be any voltage from -3 to -14 for a desired output swing.

Figure 21. Typical Application. 512 x 12 MM5203 memory.

Programming the MM5203

The MM5203 normally is shipped unprogrammed, with all 2048 bits initially in the "1" state (output high). Information is introduced by selectively programming "O"s (output low) in the proper bit locations.

Word addresses are selected by the same decoding circuitry used in the Read mode. Addresses must be present at least 1 μs before the program pulse is applied. Use the eight output terminals as data inputs to determine the information pattern in the eight bits of each word. A low data-input level (-50V) will program a "1"; a high data-input level will leave a "O".

Setting the desired bit information patterns on the data input terminals programs all eight bits of a word simultaneously. The duty cycle of the V_{DD} pulse (amplitude and width as shown in Figure 19) should be limited to 2%. National recommends putting a fan on the part for faster and better programming.*

In program mode, data inputs 1-8 are pins 4-11 respectively, regardless of the logic state of A_9 and mode control. Chip Select should be disabled (high).

Positive logic is used during the read mode for addresses and data out. Address O corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "O" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address O corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" at a data input corresponds to V_{ILP}. A "O" at a data input corresponds to V_{IHP}.

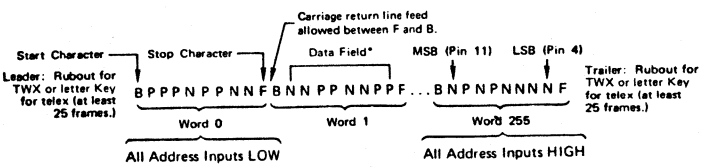
MODE	DATA AND ADDRESS LINES HIGH	DATA AND ADDRESS LINES LOW	V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
Read	V_{SS} - 2.0	V_{SS} - 4.0	+5	V_{SS}	-12	V_{SS}	V_{SS} - 4V	-3V to -12V
Program	V_{SS} -2.0	V_{SS} - 40	GND	+12	-48 (Pulse)	-48 (Pulse)	GND	GND to -50V

Erasing Procedure

The MM4203Q/MM5203Q may be erased by exposure to short-wave ultraviolet light-253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2 i.e., if the device appears erased after 8 minutes, continue exposure for an additonal 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-2 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4203/MM5203 should be placed about one inch away from the lamp for about 20-30 minutes.

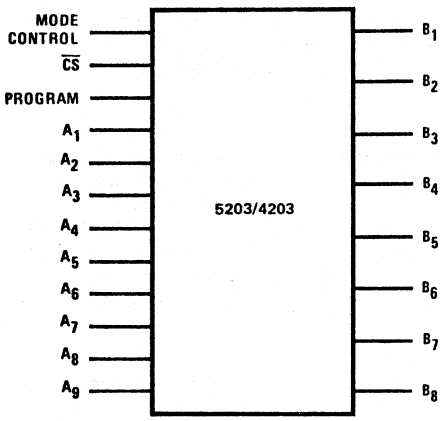
Preferred Tape Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:

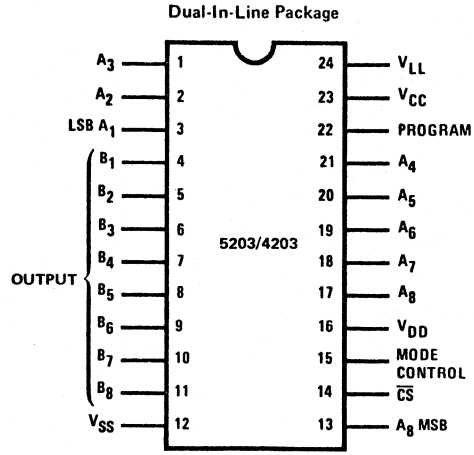


*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

*Critical voltages for the MM5203 are $V_{BB} = +12$ and $V_{PROG} = -49V \pm 1V$.



Logic Symbol



Pin Assignment

A1 – A9	Address Inputs
$\overline{CS}$	Chip Select Input
$B_{out}1 - B_{out}8$	Data Outputs

FIGURE 13. Logic and Pin Configuration – 5203

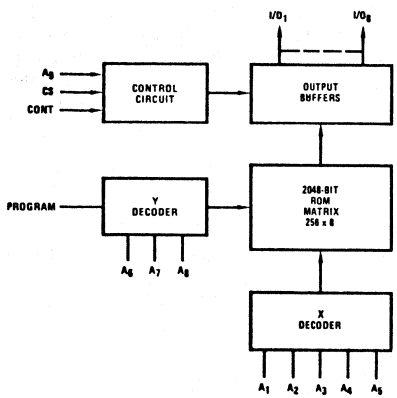


FIGURE 14. Block Diagram – 5203

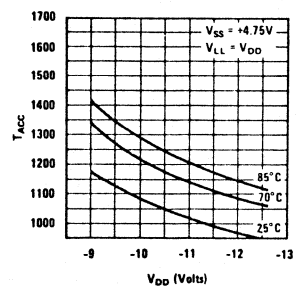


FIGURE 15. Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage – 5203

TABLE F. Electrical Characteristics –5203

a. dc.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_{LI}	Input Current	V_{IN} = 0V			1	μA
I_{LO}	Output Leakage	V_{OUT} = 0V, CS = V_{SS} = 2.0			1	μA
I_{SS}	Power Supply Current	T_A = 25°C, CS = V_{SS} = 2.0		35	55	mA
V_{IL}	Input LOW Voltage		V_{SS} - 10		V_{SS} - 4.0	V
V_{IH}	Input HIGH Voltage		V_{SS} - 2.0		V_{SS} + .3	V
V_{OL}	Output LOW Voltage	1.6mA sink -12.6V ∂ V_{LL} ∂ -3V			.40	V
I_{CF}	Output Clamp Current	V_{LL} = -3.0V, V_{OUT} = -1.0V, T_A = 0°C		3.5	6.0	mA
		V_{LL} = -12.6V, V_{OUT} = -1.0V, T_A = 0°C		8.0	15.0	mA
V_{OH}	Output HIGH Voltage	0.8mA source	2.4			V

b. ac.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
T_{OH}	Data Hold Time	(Min. Access Time) Figure 8			100	ns
T_{ACC}	Access Time	T_A = 25°C Figure 8		700	1	μs
T_{CO}	Chip Select Time	Figure 8			500	ns
T_{OD}	Chip Deselect Time	Figure 8			500	ns
T_{CS}	Allowable Chip Select Delay	Figure 8 – Allowable delay in selecting chip after change of address without affecting access time.			100	ns

c. capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
C_{IN}	Input Capacitance	V_{IN} = V_{SS} } F = 1.0 MHz		8	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = V_{SS} } CS = V_{SS} - 2.0		8	15	pF

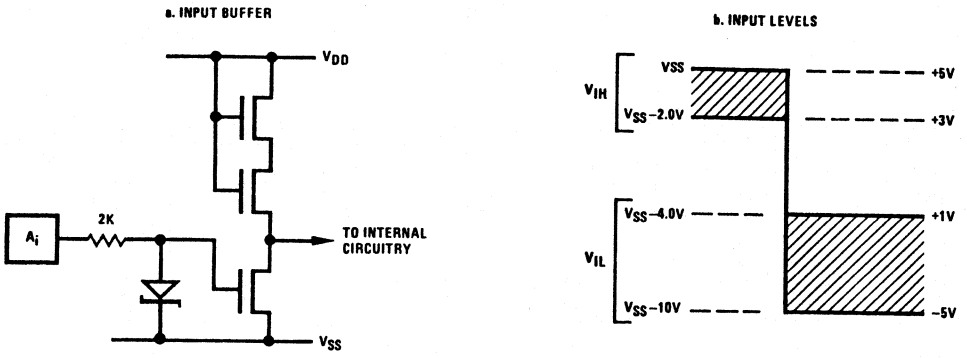
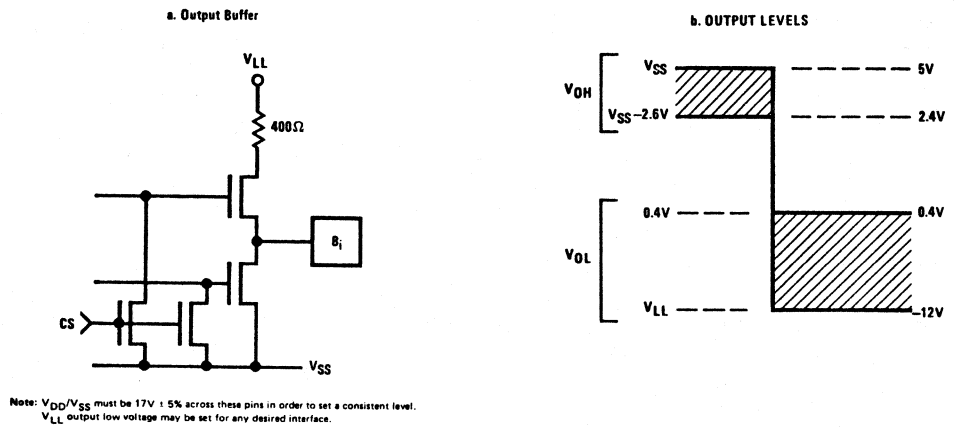


FIGURE 16. Input Characteristics – 5203



Note: V_{DD}/V_{SS} must be 17V ± 5% across these pins in order to set a consistent level.
V_{LL} output low voltage may be set for any desired interface.

FIGURE 17. Output Characteristics – 5203

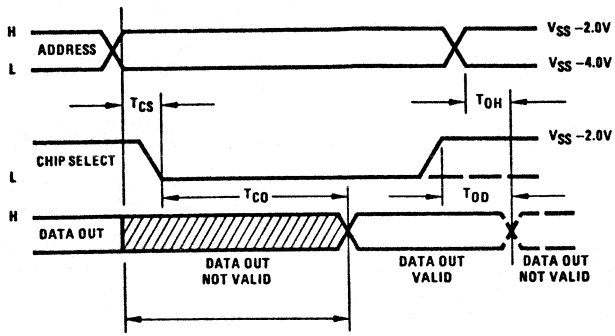


FIGURE 18. Read Operation Timing — 5203

TABLE G. Read Conditions — 5203

Pin	HI	LO	COMMENTS
ADD	V_{SS} to V_{SS} –2V	V_{SS} –4V to V_{SS} –10V	Address 0 is all Add @ V_{IL} — Address 255_{10} is all Add @ V_{IH}
DATA Outputs	V_{SS} to V_{SS} –2V	V_{LL} to .4V	
CS	V_{SS} to V_{SS} –2V	V_{SS} –4V to V_{SS} –10V [Enable Outputs]	
PROG	V_{SS}	–	
V_{DD}	–	–12V ± 5%	55mA Max.
V_{SS}	–5V ± 5% (Reference)	–	55mA Max.
V_{BB}	+5V ± 5%	–	
V_{LL}	–3V to –12V		Effects Output Voltage on LOW ONLY
MODE CTL	V_{SS} 256 X 8 mode	GND or V_{DD} 512 X 4 mode	
A9 512 X 4 mode	V_{SS} Odd Outputs 'ON'	GND or V_{DD} Even Outputs 'ON'	

2

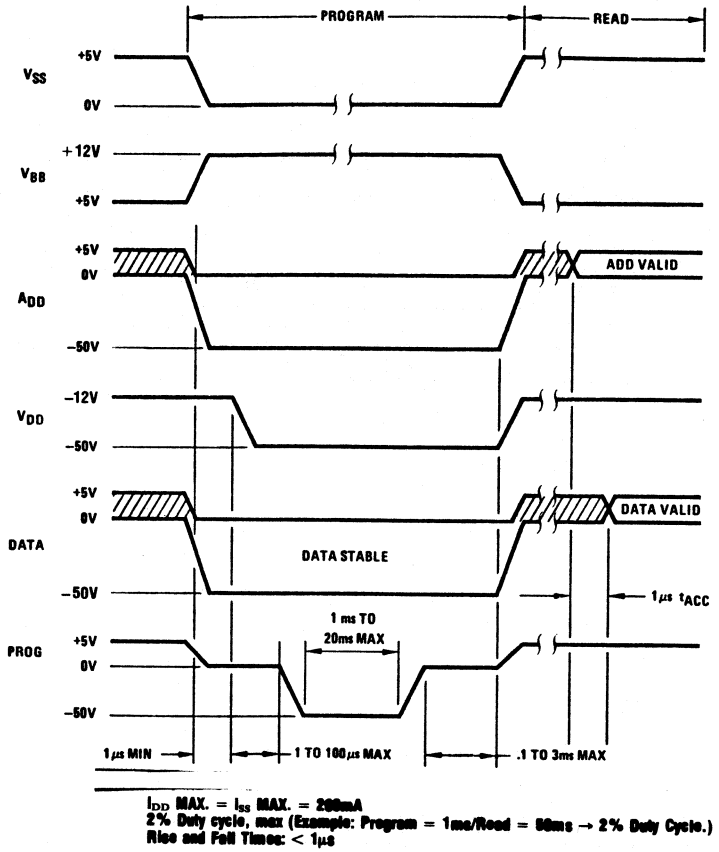
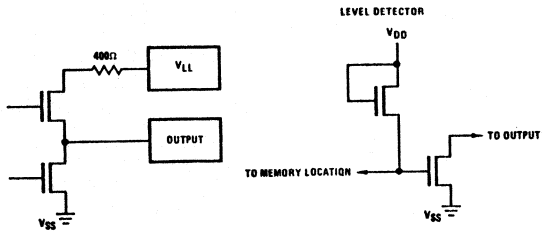


FIGURE 19. Program Waveforms – 5203

TABLE H. Program Conditions – 5203

Pin	HI	LO	MAX I	COMMENTS
ADD	V_{SS} to V_{SS} –2V	V_{SS} –40V to V_{SS} –50V	10mA	
DATA	V_{SS} to V_{SS} –2V	V_{SS} –40V to V_{SS} –50V	10mA	HIGH – Leaves Unprogrammed LOW – Allows Programming
CS	0V (V_{SS})	–	–	MUST be LOW
PROG	0V (V_{SS})	–48V to –50V	10mA	*
V_{DD}	0V (V_{SS})	–48V to –50V	1000mA	2% duty cycle MAX.
V_{SS}	0V (Ref)	–	1000mA	
V_{BB}	+12V	–	100mA	
V_{LL}	$0 \leq V_{LL} \leq -50$		–	Not used during programming
MODE CTL	V_{SS} –2.0 or V_{SS} –4.0		–	Not used during programming
A9	V_{SS} –2.0 or V_{SS} –4.0		–	Not used during programming

*Program time is the amount of time the program pin is low (–49V ± 1V).
Fixed-time program is 200ms, or X + AX where A = 3 and X = V_{PROG} pulse width.
(Pulse width may be 20ms maximum.)



DESIRED OUTPUT SWING CMOS	SUPPLY VOLTAGES	OUTPUT SWING
6V	V_{SS} = 5, V_{DD} = −12, V_{LL} = GND	V_{OH} = V_{SS} = +5 V_{OL} = V_{LL} = GND (Never Move Neg)
10V	V_{SS} = +10, V_{DD} = −7, V_{LL} = GND	V_{OH} = +15 V_{OL} = GND TO GND +2V (Never Move Neg)
15V	V_{SS} = +15, V_{DD} = −2, V_{LL} = GND	V_{OH} = +15
+5, −7	V_{SS} = +5, V_{DD} = −12, V_{LL} = −7	V_{OH} = +5 V_{OL} = −7

FIGURE 20. Output Structure — 5203

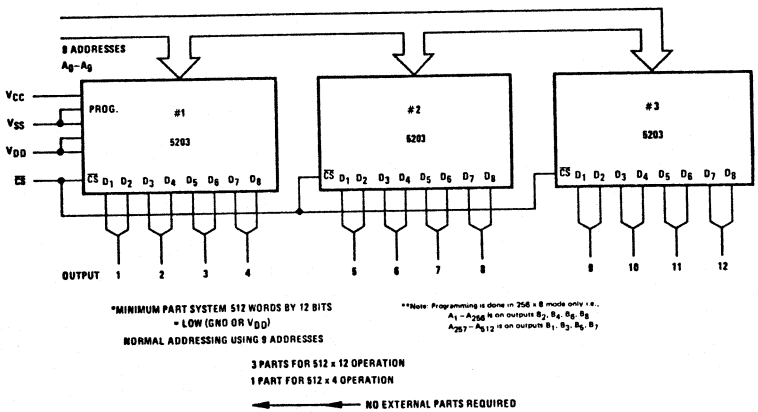


FIGURE 21. Typical Applications

3. The MM5204 EPROM

(Milltary specification version: MM4204)

The National MM5204 is a 4096-bit ROM that is electrically programmable and is erasable by ultraviolet light. It is organized as 512 words of 8 bits each.

In addition to the features shared by the MM1702 and MM5203, the MM5204 includes a logic input called "Power Saver," which provides a 5-to-1 decrease in power when the memory is not being accessed. "Power Saver" is also well suited for low-power applications.

The following figures and tables illustrate the structure, operating characteristics and programming characteristics of the National MM5204.

Structure

Figure 22. Logic and Pin Configuration.

Figure 23. Block Diagram.
Logic Symbol.
Pin Assignment.
Pin Names.

Operating Characteristics

Table I. Electrical Characteristics.
a. dc.
b. ac.
c. capacitance.

Figure 24. Input Characteristics.
a. Input buffer. PS is Pwr Svr . . unique to the MM5204.
b. Input levels.

Figure 25. Output Characteristics.
a. Output buffer.
b. Output levels.

In the case of the MM5204, V_{LL} must equal V_{SS}-5V±5%. This differs from the MM1702, which has no V_{LL} number, and from the MM5203, which has a V_{LL} range.

This may also be expressed:

$V_{LL}=(V_{SS}-4.75)$ to $(V_{SS}-5.25)$. It is essential for proper access times.

Figure 26. Read Operating Timing. V_{SS} to V_{LL} read voltage is the most critical of all supplies. See information with Figure

Figure 27. Access Time vs. V_{DD} and Temperature.

Table J. Read Conditions.

Figure 28. Power Saver Timing.

Additional notes about the MM5204 Power Saver.

P.S. high will put the part in question into Tri-State regardless of current-supply voltage. Supply current will then move from 40 mA maximum (0°C in the MM5204) to 8 mA maximum.

Timing from Power Saver low to outputs valid is specified at 1.8 μs maximum.

Typically, if addresses are changed after the Power Saver is low, then the time to outputs valid is the same as the 1-μs access time of the part (or t_{acc} as indicated in Figure 28). When addresses are not changed after the Power Saver is low, then the time to outputs valid will be the same as the 1.8μs setup time (or as indicated in Figure 28).

Power Saver must be at V_{SS} during programming. Power saving concept valid during read/standby only (not programming).

Figure 29. Program waveforms.

Table K. Program conditions.

Programming the MM5204

The MM5204 normally is shipped unprogrammed with all 4096 bits in the "O" logic state. (Refer to the tables of programming characteristic and program conditions.) In the program mode the MM5204 effectively becomes a RAM, with the 512 word locations selected by address inputs AO-A8. Write operation for data input is controlled by pulsing the program input. Since the MM5204 is shipped unprogrammed, a V_{IHP} on any data input will leave the stored "0"s undisturbed, and a V_{ILP} on any data input will write a logic "1" into that location.

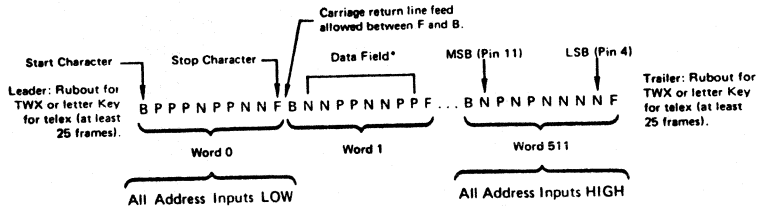
If the customer prefers the EPROM preprogrammed, data may be submitted to National Semiconductor for factory programming.

One of the following formats should be used:

Figure 30. A typical application.

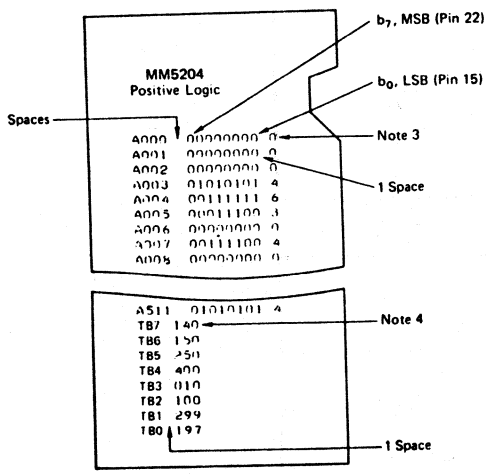
preferred format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

alternate format [Punched Tape (Note 1) or Cards]

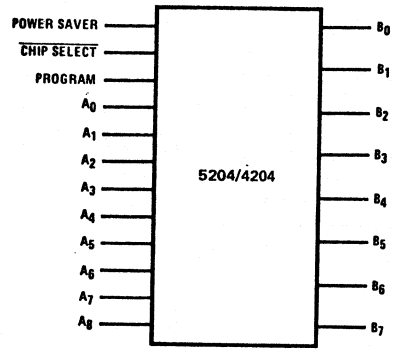


Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

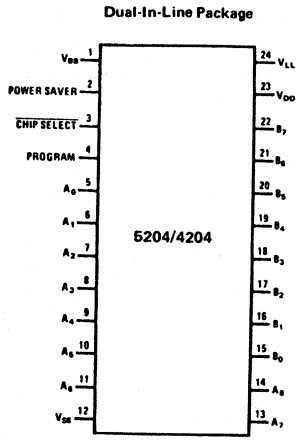
Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.



Logic Symbol



Pin Assignment

Pin Names

A0 – A8	Address Inputs
$\overline{CS}$	Chip Select Input
$B_{out}0 - B_{out}7$	Data Outputs

FIGURE 22. Logic and Pin Configuration – 5204

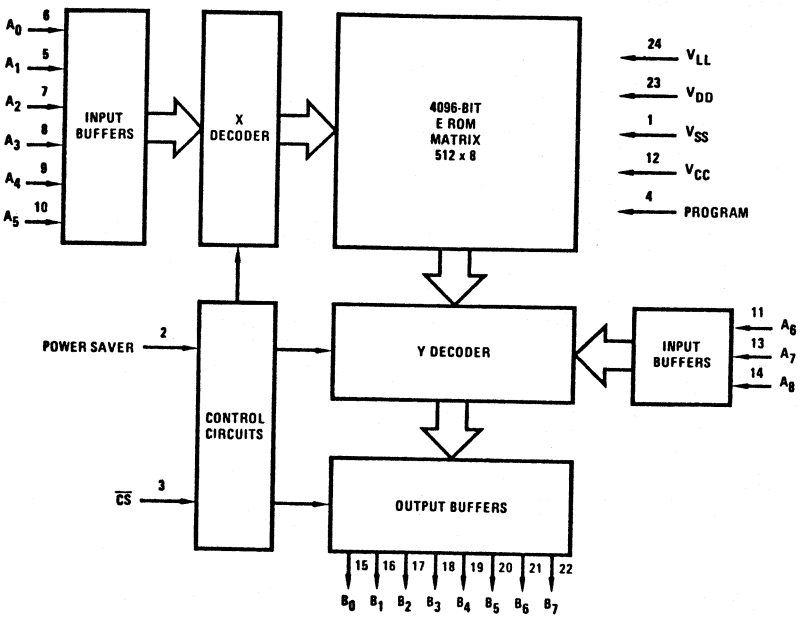


FIGURE 23. Block Diagram – 5204

TABLE I. Electrical Characteristics — 5204/4204

a. dc.

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10.0	mA
I_{SS}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

b. ac.

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5.0V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5.0V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C, *(Figure 1)*, (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, *(Figure 1)*, (Note 4)			1.25	μs
t_{PO}	Power Saver Set-Up Time					
	MM5204	*(Figure 1)*			1.8	μs
	MM4204	*(Figure 1)*			2.0	μs
t_{CO}	Chip Select Delay					
	MM5204	*(Figure 1)*			500	ns
	MM4204	*(Figure 1)*			600	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
t_{ODP}	Power Saver Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns

c. capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

2

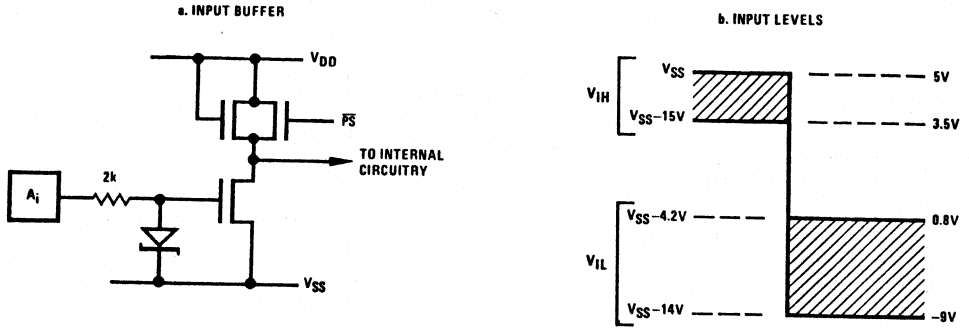


FIGURE 24. Input Characteristics – 5204

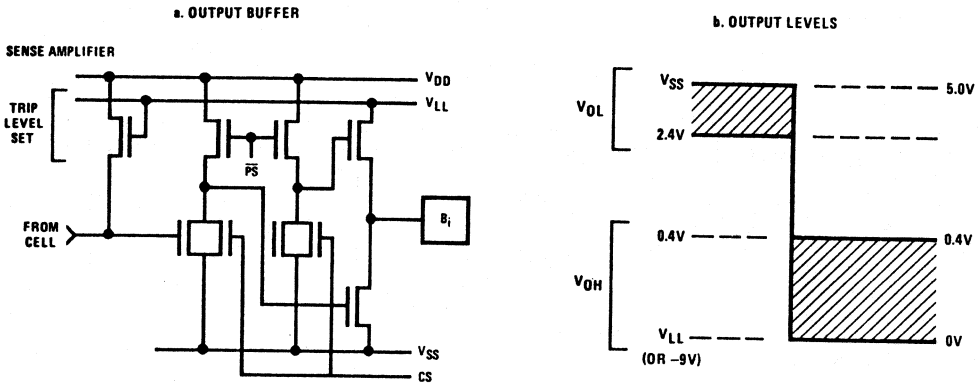


FIGURE 25. Output Characteristics – 5204

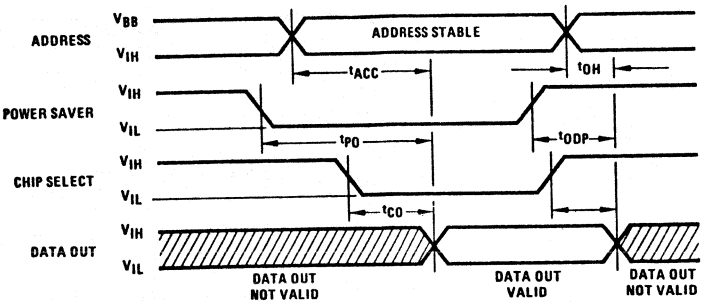


FIGURE 26. Read Operation Timing – 5204

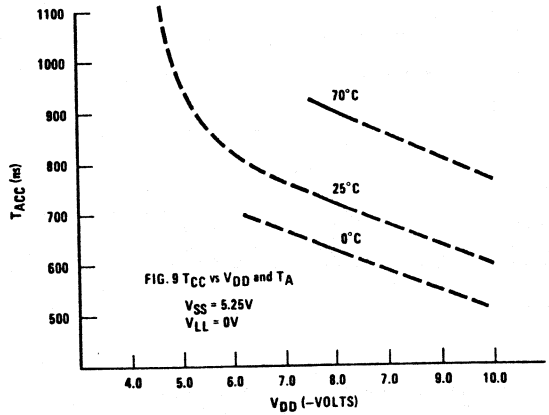
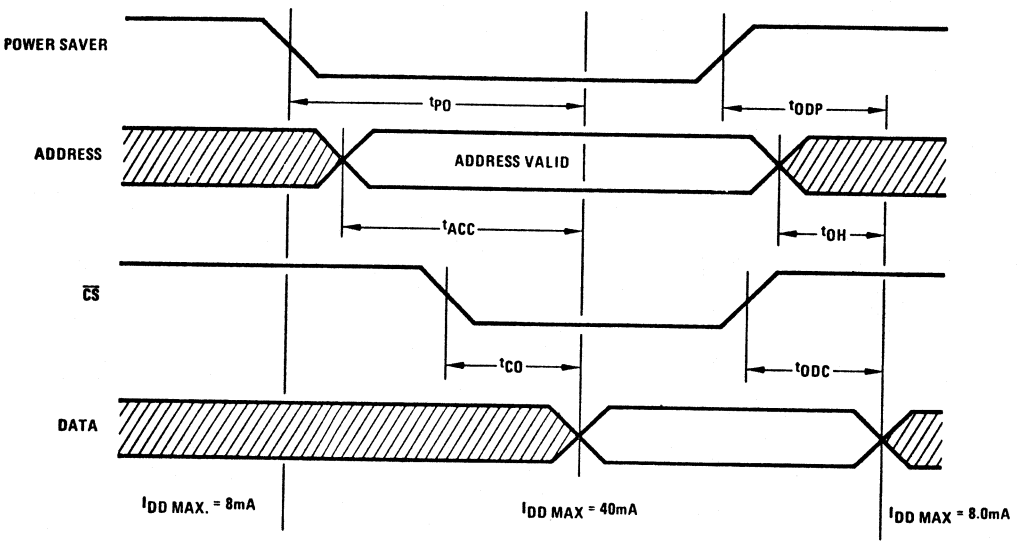


FIGURE 27. Access Time Vs. Vpp and Temperature – 5204

2

TABLE J. Read Conditions – 5204

PIN	HIGH	LOW	COMMENTS
ADD	V_{SS} –1.5V to V_{SS}	V_{SS} –4.2V to V_{SS} –14V	
DATA Outputs	2.4V to V_{SS}	V_{LL} to .4V	
CS	V_{SS} to V_{SS} –1.5V Outputs TRI-STATE	V_{SS} –4.2V to V_{SS} –1.4V [Outputs ENABLED]	
P.S.	V_{SS} to V_{SS} –1.5V Outputs TRI-STATE	V_{SS} –4.2V to V_{SS} –14V	P.S. LOW – I_{DD} = 8mA – TRI-STATE Outputs
PROG	V_{SS}	–	
V_{LL}	0V (V_{SS} –5V)	–	V_{LL} to V_{SS} Voltage
V_{SS}	+5V ±5%	–	Very CRITICAL
V_{DD}	–	–12V ± 5%	I_{DD} MAX = I_{SS}MAX = 40mA
V_{BB}	+5V ± 5%	–	



t_{PO} = Power Saver setup time: 1.8 μs maximum.
t_{ACC} = Access time: 1.0 μs maximum.
t_{CO} = Chip select delay: 0.5 μs maximum.
t_{OH} = Data hold time: 30 ns min.
t_{ODP} = Power Saver deselect time: 30 ns min. (500 ns maximum)
t_{ODC} = Chip select deselect time: 30 ns min. (500 ns maximum)

T_A within operating temperature range. V_{LL} = 0V.
V_{BB} = V_{SS}. MM4204: V_{SS} = 5.0V ± 10%, V_{DD} = –12V ±5%.
MM5204: V_{SS} = 5.0V ± 5%, V_{DD} = –12V ± 5%.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{PO}	Power Saver Set-up Time		1.8	μs
t_{ACC}	Access Time		1.0	μs
t_{CO}	Chip Select Delay		0.5	μs
t_{OH}	Data Hold Time	30		ns
t_{ODP}	Power Saver Deselect Time	30	500	ns
t_{ODC}	Chip Select Deselect Time	30	500	ns

FIGURE 28. Power Saver Timing – 5204

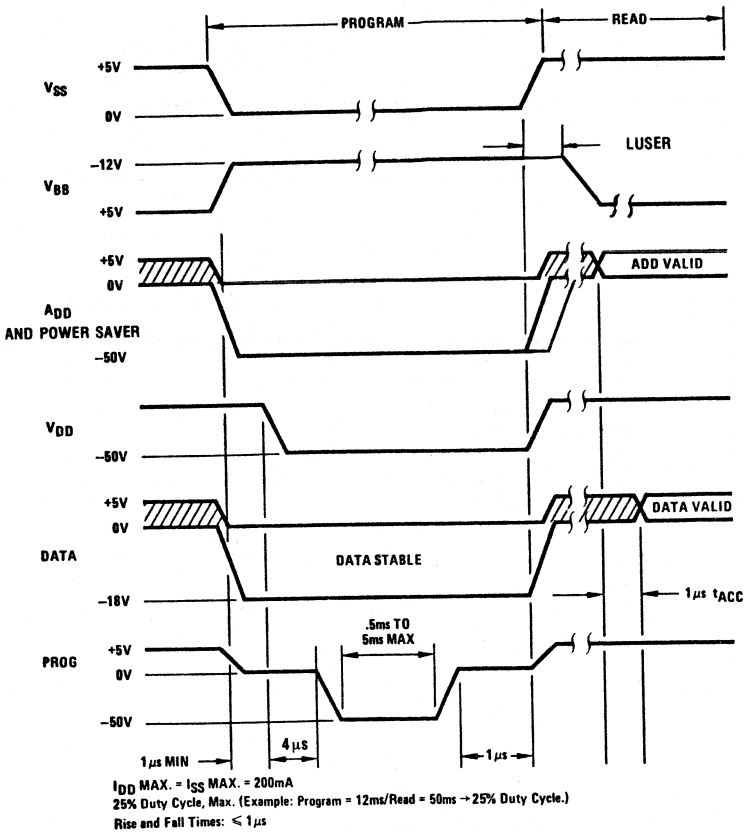


FIGURE 29. Program Waveforms — 5204

TABLE K. Program Conditions — 5204

PROGRAM CONDITIONS

PIN	HI	LO	MAX I	COMMENTS
ADD	V_{SS} to V_{SS} −2V	V_{SS} −11V to V_{SS} −50V	10mA	
DATA	V_{SS} to V_{SS} −2V	V_{SS} −11V to V_{SS} −18V	10mA	HI – Will Leave Unprogrammed LOW – Will Program
CS	V_{SS}	–	–	Outputs must be unenabled
P.S.	V_{SS}	–	–	Power Saver must be @ V_{SS} or Current Flow will be Very Great
PROG	V_{SS}	V_{SS} −48V to V_{SS} −50V	10mA	*
V_{LL}	0V to −14V	–	100mA	
V_{SS}	0V (Ref)	–	200mA	
V_{DD}	V_{SS}	V_{SS} −48V to V_{SS} −50V	200mA	25% duty cycle – MAX
V_{BB}	+12 ±5%	–	100mA	

***Program time** is the amount of time the program pin is low (−49V ± 1V).
Fixed-time program is 100ms or X + AX where A= 5 and X= V_{PROG} pulse width.
(Pulse width may be ;.5ms or 5.0ms maximum.)

2

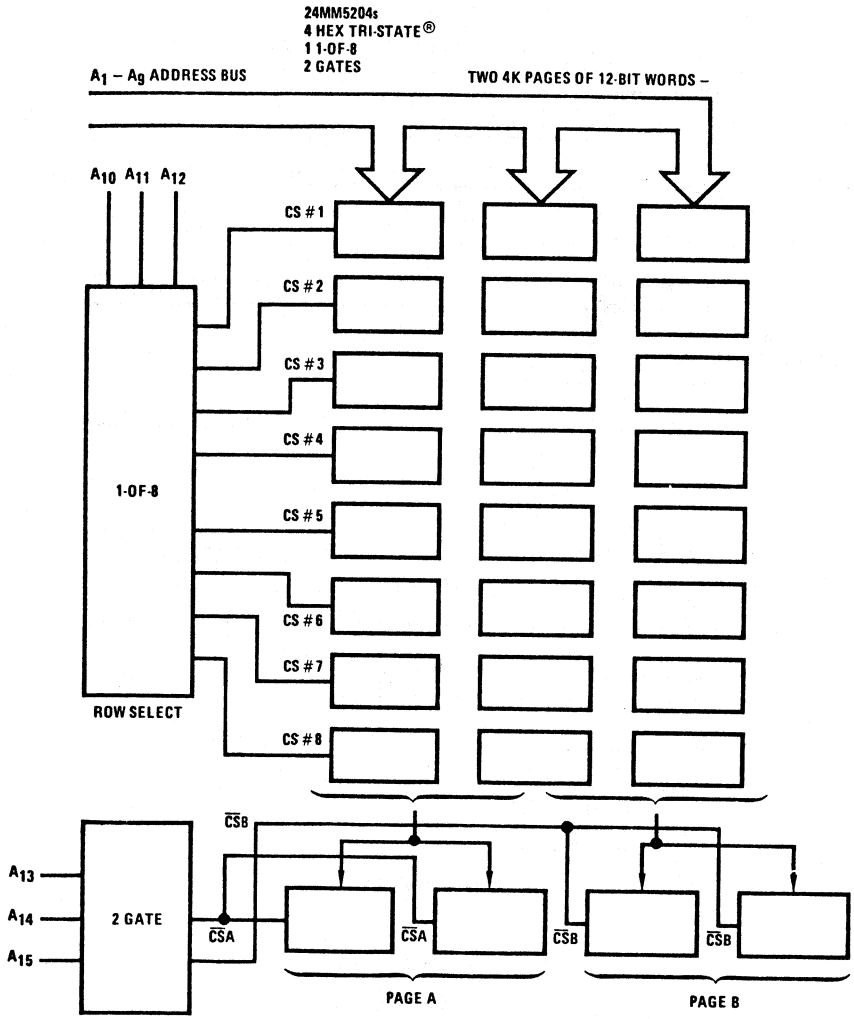


FIGURE 30. A Typical Application (without all connection lines)

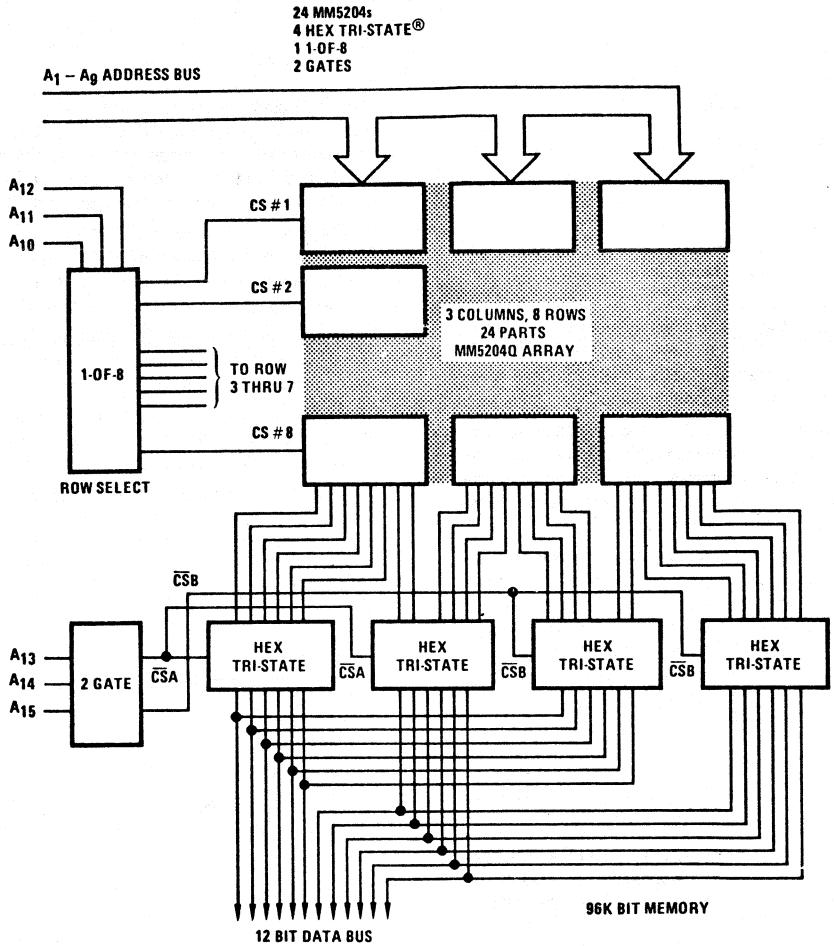


FIGURE 30. A Typical Application (with Details)

SECTION III
APPLICATION OF NATIONAL EPROMs.

1. System requirements.

To design EPROMs into systems successfully requires special considerations. For example:

Ambient Light.

Cover the transparent EPROM lid with an opaque material during program and read operations.

Normal ambient lighting does not contain enough ultraviolet light to discharge the floating gate in the FAMOS cell and erase data. But there may be enough UV-generated photocurrent to upset the finely balanced sense amplifier and even the decode circuits.

This could cause problems that are often difficult to diagnose. Such problems may include changes in access times and in output states, programming of extra bits, and false reading of the programmed state. The last item can lead to insufficient programming of the parts.

EPROMs are sensitive to temperature. In designing EPROMs into systems, it is important to know how much higher the chip temperature is than the ambient system temperature, often called the chip-temperature overage. Figure 36 in the Appendix presents a formula for determining the true chip-temperature overage to use in de-rating calculations of minimum data retention time.

Voltage

– Keep the voltage lines as short as possible and well filtered. –

EPROMs have plus and minus voltages, yet no ground is supplied. Therefore, one of the voltages becomes the reference, and the regulation and distritibution of the voltages becomes critical.

It must be remembered that MOS devices are voltage-sensitive. Also, the voltage thresholds of p-channel devices (such as National EPROMs) are relative to V_{SS}. When shared with the V_{CC} of a bipolar system, the V_{SS} is subject to large current swings, which cause voltage noise.

2. Interfacing EPROMs with Other Logic Families.

When using EPROMs in mixed logic families, considerations arise in the areas of interfacing and (as a consequence) speed.

Such matters as input currents and output capability are covered clearly in National data sheets, and adhering to the values given in the data sheets will generally prevent errors in current loading.

One potential problem is capacitive overloading, which reduces the speed of the system.

The MOS output structure has a much higher im-pedance than does the current source/sink of a bipolar device. Because of this, the driven capacitance determines the propagation delay. More importantly, the capacitance plays a greater role in determining rise and fall times in a MOS device that it does in a bipolar device.

The use of Tri-State outputs makes the building of memory arrays easier, because the unselected devices are allowed a state of high impedance. This is made possible by simply turning off both source and sink transistors of each output.

Even in a state of high impedance, of course, the output does add a capacitance to the bus line.

This illustrates the overall rule that capacitive loading of "off" devices, along with other parasitic loads, must always be considered when timing becomes critical.

It must be remembered that different logic families have different thresholds and voltage restrictions. For example, some fast devices, such as some bipolar circuits are prone to oscillate with slow rise and fall times. At times, achieving compatibility may require additional interface elements.

Figures 31,32 and 33. Three interfacing examples, using EPROMs, in system design. These are applicable to all National EPROMs.

Figure 31. CMOS,single supply interfacing.

Figure 32. Dual supply interfacing.

Figure 33. Dual supply interfacing of bipolar/MOS system.

3. Production environment requirements.

Considerations unique to the use of EPROMs in a production environment arise from the program and erase functions of the devices. These functions are interdependent, so always check both functions, not just one, when investigating EPROM performance.
Production considerations include:

1.) Special Handling.

MOS devices with quartz lids are fragile and subject to static charge damage as well as mechanical damage. They are to be stored in boxes with the leads embedded in conductive foam or in non-static rails, with foam rubber at the ends to protect them from mechanical shock.

2.) Calibrate Programmers Weekly and Ultraviolet Lamps Monthly.

Poor data retention may be due to a programmer that is out of specification in voltage or timing. It may also be due to incomplete erasure by a UV lamp previous to the present programming.

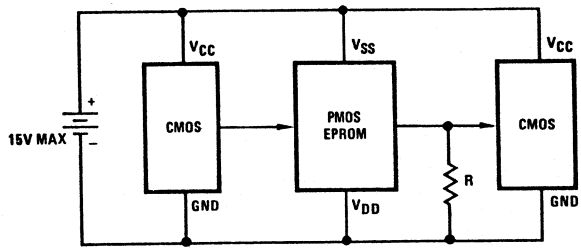
If the programmer is operating properly, and if erasure is complete (x + 2x, as explained in Section I), then program yields greater than 99 percent are to be expected. Yields less than 96 percent are a sure indication of a malfunction.

3.) Maintain Records of Parts Problems.

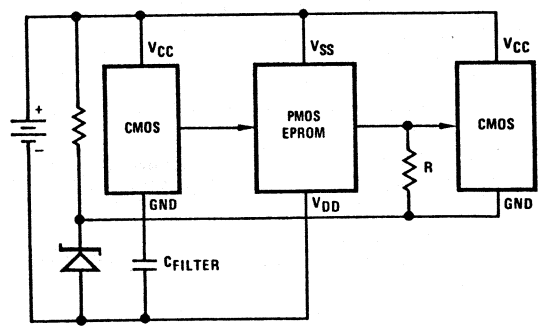
A good bookkeeping routine, provides histories of parts problems, is necessary for successful troubleshooting of any system. Continued program rejects, for example, may be due simply to a worn-out socket. Part failure may also be responsible when an output appears to be continually programmed yet will neither provide complete data nor erase.

4.) Place an Opaque label in the Quartz Lid.

This protects the EPROM from accidental UV erasure and from disturbing photocurrents in ambient light. It also provides a convenient place to record pattern identification and programming data.



SINGLE SUPPLY < 15V



SINGLE SUPPLY = $|V_{DD}| + |V_{SS}|$

FIGURE 31

2

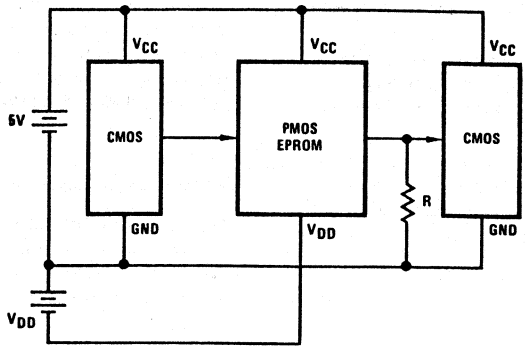


FIGURE 32. Dual Supply Interfacing – CMOS

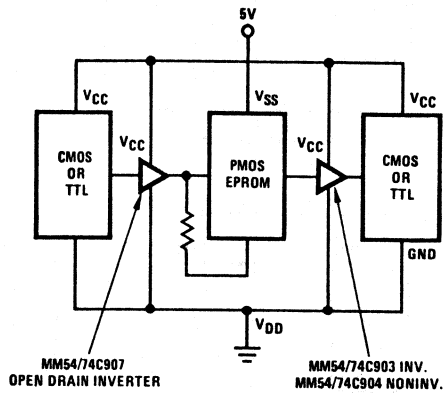


FIGURE 33. Dual Supply Interfacing of Bipolar/MOS System

APPENDIX

Figure 34.

Floating gate of a FAMOS cell in three conditions:

a.) Equilibrium. Charge on floating gate is very near zero; no conductance from source to drain is possible except at high voltage.

b.) Programming. Very high negative voltage is applied to drain. Electrons are being avalanche-injected to the floating gate.

c.) Data retention. Voltage is discontinued. But because the floating gate is surrounded by oxide, the charge stays on the gate. Accordingly, conductance may be detected between the source and the drain.

Figure 35. Erasing data from a FAMOS cell.

High-intensity ultraviolet light strikes near the polysilicon floating gate. The resultant photocurrent energizes the stored electrons and excites them over the silicon dioxide "wall", thus discharging the floating gate.

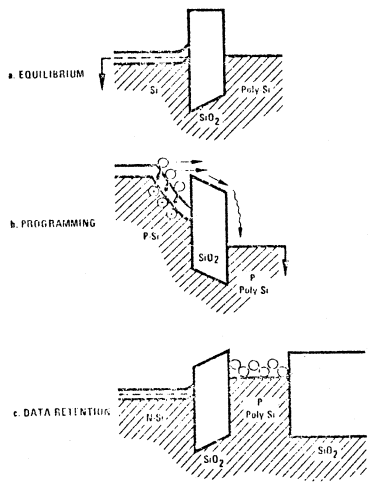


FIGURE 34. FAMOS Cell in Three Conditions.

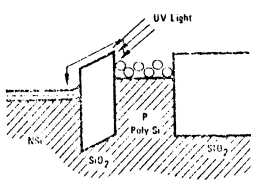


FIGURE 35. Erasing Data from a FAMOS Cell

Table L. Programmers for use with National EPROMs.

These ready-to use instruments have been evaluated and approved by National. They range from single-device, single-unit models through multi-unit copiers, to versatile multi-device programmers.

NAME	EPROMs VERIFIED
Data I/O	All
Prolog	All
PROM Prpgrammers	All
Spectrum Dynamic	1702A Only
SC/MP LCDS 5204 Programmer	5204 Only

Table M. Ultraviolet lamps for use with National EPROMs.

Ultraviolet products S-52
Turner products UV erase lamp
GE germicidal bulbs 4 inch to 6 inch

Table N. Recommended procedure for calibrating ultrviolet systems.

The steps for calibrating ultraviolet erase systems are:

1. Configure the system (type of bulb, distance etc.) as it will be used.
2. Select a sample of the device type (a minimum of 10 parts)
3. Fully program the parts
4. Erase/test, Erase/test, until testing indicates erasure is just barely complete and record the total erase time of each part.
5. Average the erase times and use 3 times that average time as standard erase time for that device type.

Calibration monthly is recommended because bulbs lose intensity as they age. Calibrate for each part type. Calibrate whenever something is changed (bulb, distance etc.)

Figure 36. Determining the true chip temperature overage to use in de-rating calculations of minimum data-retention time.

The thermal resistance of the system package is symbolized by ϕjA.

It is expressed in the degrees by which the chip temperature is higher than that of the still air surrounding the package per watt of power consumed in the circuit.

As an example:

ϕjA = 40°C/watt, V_{SS} = 5 volts, V_{DD} = -10 volts,

I_{DD} = 25 mA,

8 inputs, and 8 outputs. (clamp current)

Each output is sinking 8 mA from V_{ss} to Vdd 50 percent of the time, and sourcing 0,1 mA from Vss to 2,5 volts the rest of the time.

The calculations:

Idd x (Vss-Vdd) = 25 x 15.0 = 375 mW

2

+ 50% I sink x V load (internal) = ½ • 8 • 10 V. x 8 mA = 320 mW

+ 50% I source x V load (internal) = ½ • 8 • 2.5 V. x 0.1 mA = 1 mW

The total power consumed in the circuit is 696 mW.

Chip temperature overage = 40°C/watt • 0.696 = 28°C.

Figure 37. Sense amplifier in a 5204 EPROM. Illustrating trip point at which a "1" or "0" is detected. Note that the trip point is set by the V_{LL} (V_{GG}) to V_{SS} voltage.

Figures 38 and 39. Temperature sense circuits for minimum program time.

Temperature sense circuits are used to allow a programmer to operate at much higher duty cycles than specified in the data sheets. The specified duty cycles guarantees that the device temperature will not rise due to power dissipation to a point that prevents correct programming. A programmer that senses the device temperature can operate at maximum duty cycle and then pause to allow the unit to cool when it heats to a defined temperature limit.

Temperature is sensed by measuring the voltage drop across the V_{SS} to V_{BB} diode (Fig.38 & 39) at room temperature and in the middle of the program sequence.

When the voltage is <350 mV (measured at 1 mA), institute a pause in the program sequence, allowing the die to cool. Continuing to program at too high a temperature will lessen programming and thus data retention of the device.

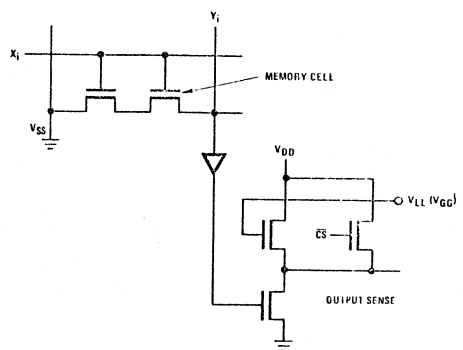


FIGURE 37. Sense Amp in an EPROM Memory Array

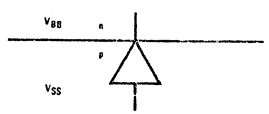


FIGURE 38. V_{SS} to V_{BB} Diode

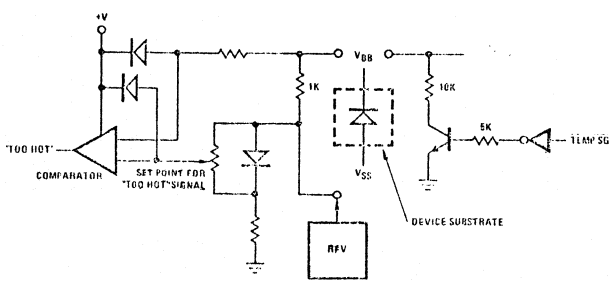


FIGURE 39. Temperature Sense Circuit

3. CHARACTER GENERATOR

National Semiconductor

Bipolar ROMs

DM8678 bipolar character generator

general description

The DM8678 is a 64-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip subtractor.

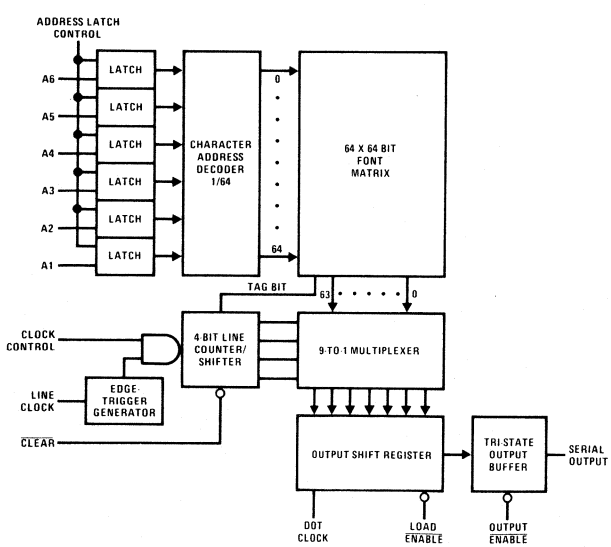
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

features

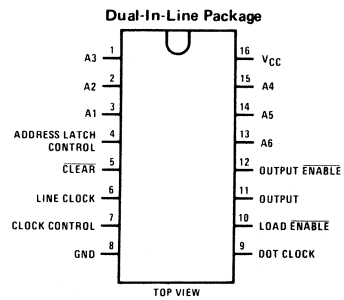
- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Shifted lower case descending characters
- Serial output
- 16-pin package
- 20 MHz clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

	ROW SCAN	7 x 9	5 x 7	FONT	PACKAGE
DM8678BWF	X	X		Upper Case Block Letters	N, J
DM8678CAE	X	X		Shifted Lower Case Block	N, J
DM8678CAB	X		X	Upper Case Block Letters	N, J
DM8678CAH	X		X	Shifted Lower Case Block	N, J
DM8678CAD	X	X		Kata Kana	N, J
DM8678BTK	X	X		Upper Case Script Letters	N, J
DM8678CAS	X	X		IBM 3741 Selectric	N, J

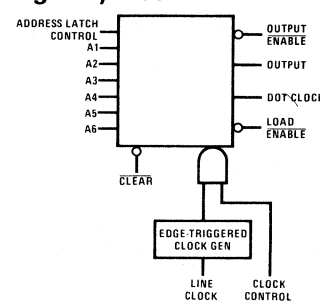
block diagram



connection diagram



logic symbol



absolute maximum ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

dc electrical characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−0.8	−1.6	mA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	145	mA
	TRI-STATE PARAMETERS					
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−50	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±40	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V

ac electrical characteristics (With standard load) (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Access Time					
T_{DO}	Dot Clock to Output			35	55	ns
T_{EA}	Output Enable			20	45	ns
T_{ER}	Output Disable			20	45	ns
	Set-Up Time					
T_{S1}	Load to Dot Clock		40	25		ns
T_{S2}	Address to Load		350	200		ns
T_{S3}	Clear to Load	See Switching Time Waveforms	350			ns
T_{S4}	Control to Line Clock		40			ns
T_{S5}	Line Clock to Load		950			ns
T_{S6}	Address to Address Latch		40			ns
	Hold Time					
T_{H1}	Load from Dot Clock		0			ns
T_{H2}	Address from Load		0			ns
T_{H3}	Control from Line Clock		100			ns
T_{H4}	Address from Address Latch		40			ns

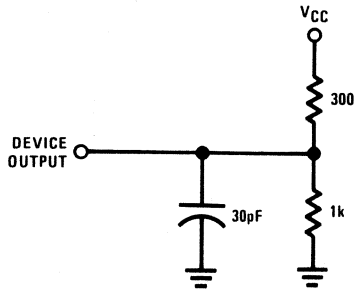
ac electrical characteristics (Continued) (With standard load) (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width					
T_{W1}	Line Clock	See Switching Time Waveforms	40			ns
T_{W2}	Clear		40			ns
T_{W3}	Dot Clock		30			ns
T_{W4}	Load		60			ns
T_{W5}	Address Latch		40			ns
f_{MAX}	Maximum Clock Frequency		16	20		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

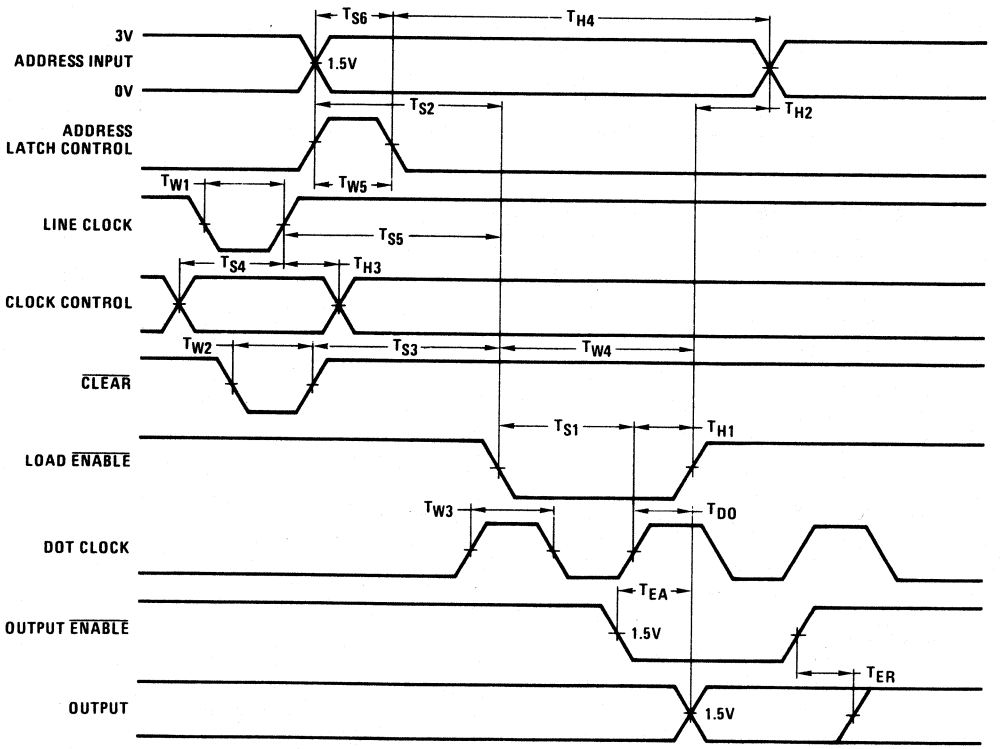
Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

standard test load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, t_r < 5 ns and t_f < 5 ns (between 1.0V and 2.0V).
- T_{DO} is measured with output enable at a steady low level.

switching time waveforms



truth tables

a) Address Latch

ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

b) Output

OUTPUT $\overline{\text{ENABLE}}$	STATE OF THE OUTPUT
1	Output Hi-Z
0	Data Out

c) 4-Bit Line Counter

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	¬	H	No change on high-to-low clock edge

X = Don't care

definitions

A1–A6: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

functional description

To select a character, a 6-bit binary word must be present at the address inputs A1–A6 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the $\overline{\text{clear}}$ input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing one horizontal line of the addressed character, is available at the output when the load $\overline{\text{enable}}$ input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out one line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low. Detailed system application infomation is contained in application note AN-167 available from National.

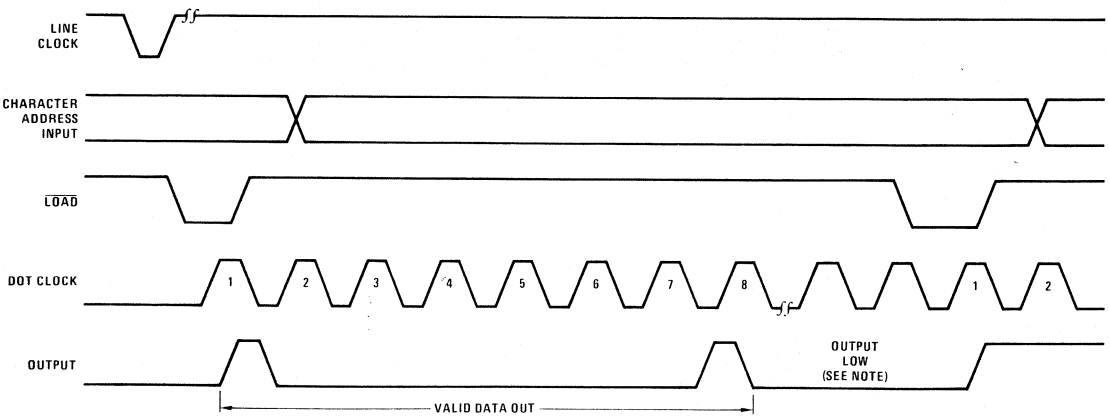
A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4.*

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10.*

functional description (Continued)

Character Cycle – ROM data corresponding to one line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

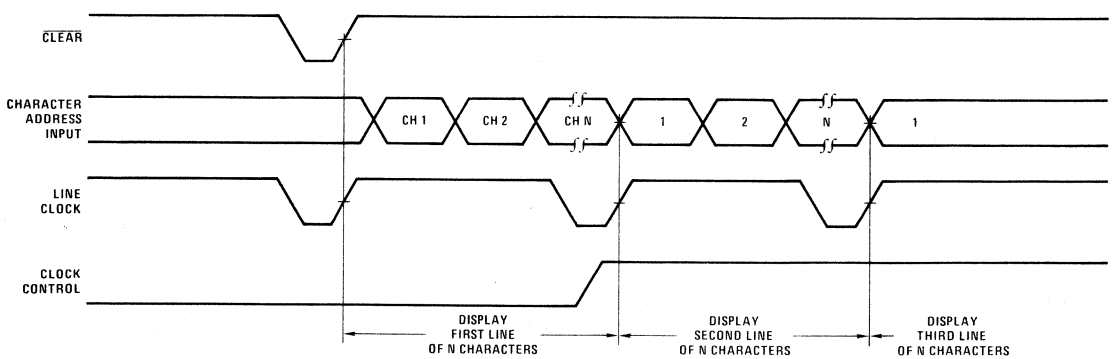


FIGURE 2. Line Cycle

functional description (Continued)

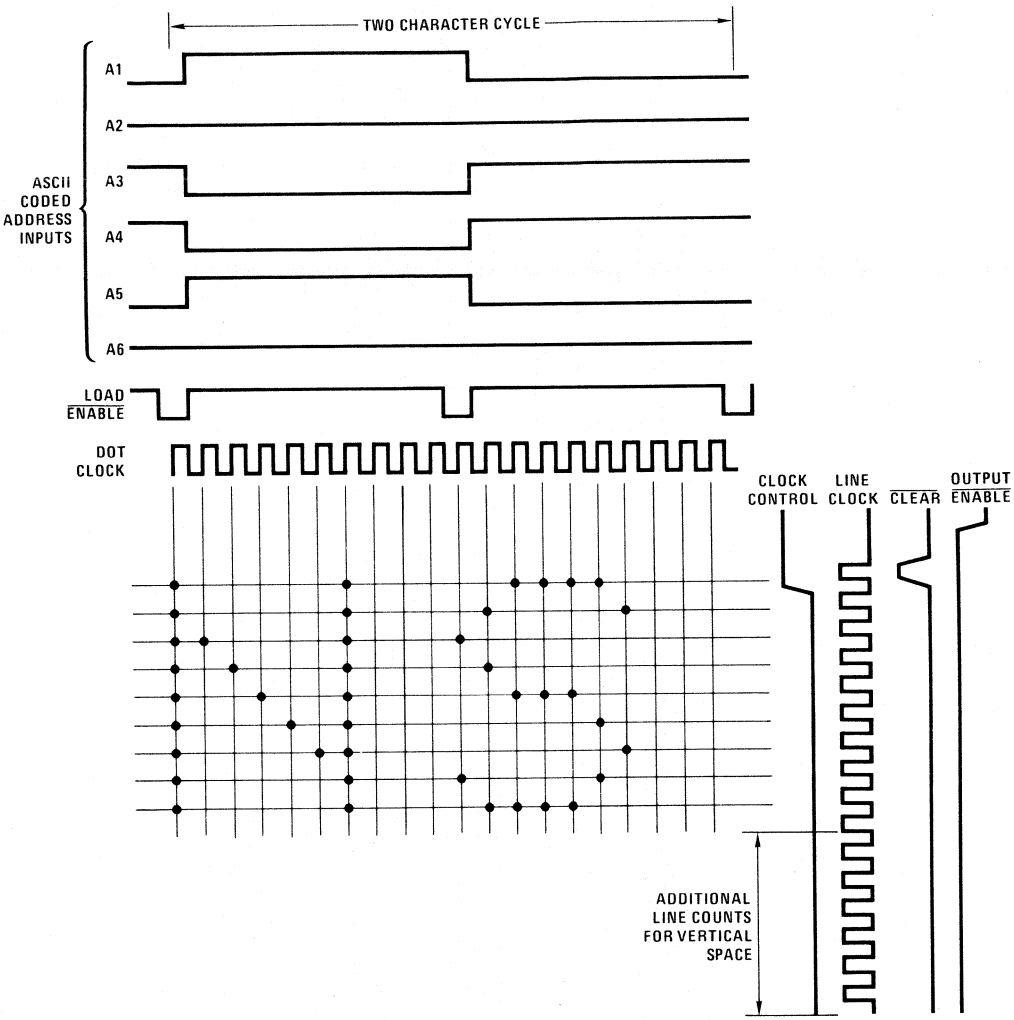
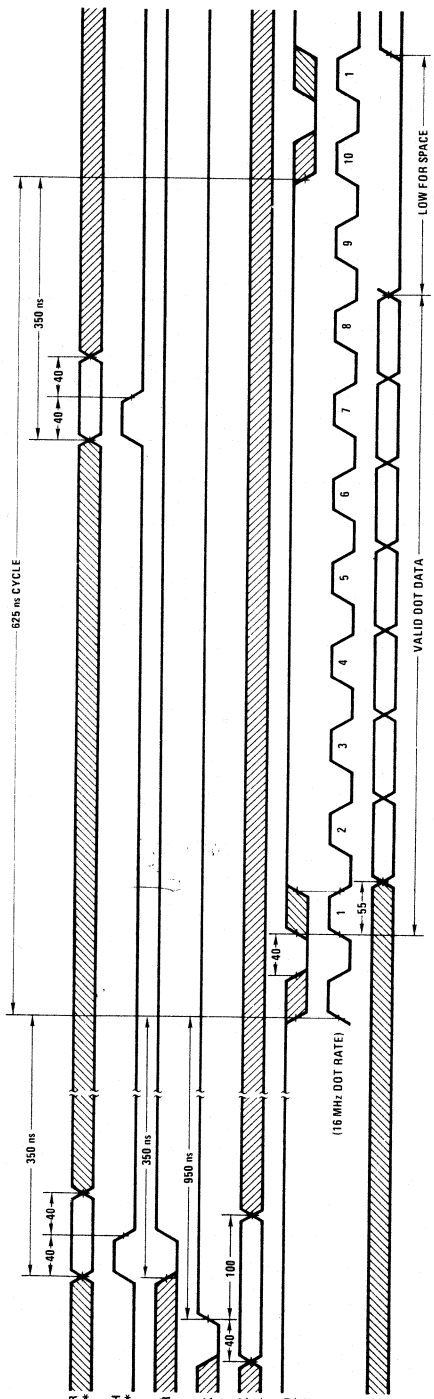


FIGURE 3. Example of Two Characters Display Timing

functional description (Continued)



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 350 ns before the high-to-low transition of Load enable.

FIGURE 4. Typical System Timing Waveform

functional description (Continued)

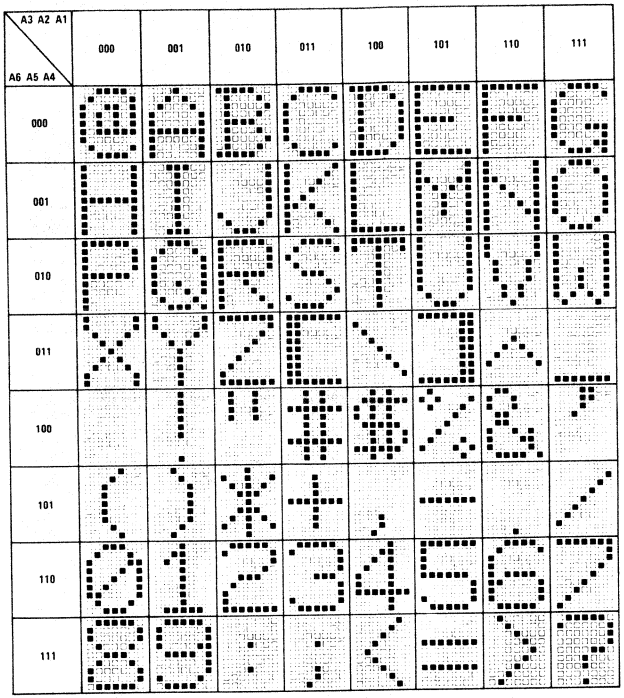
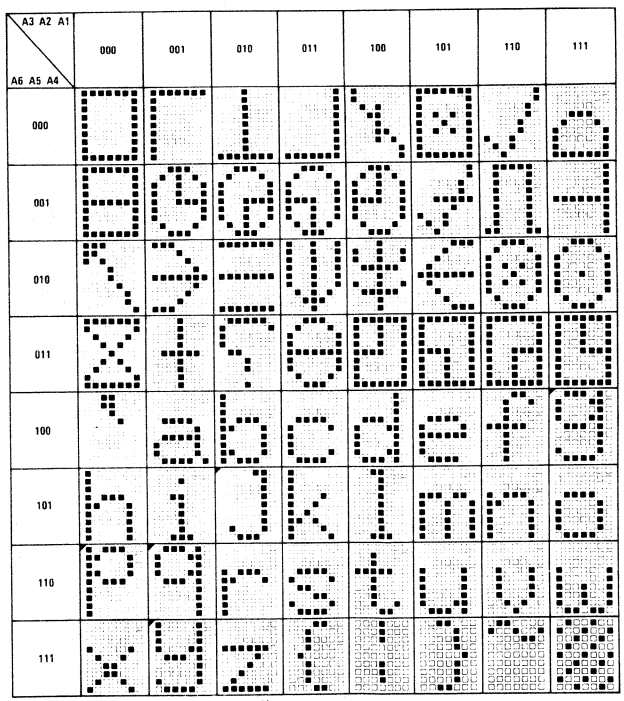


FIGURE 5. DM8678BWF



◤Shifted characters (see *Figure 12*)

FIGURE 6. DM8678CAE

Note. A "filled in" dot represents a high memory output.

functional description (Continued)

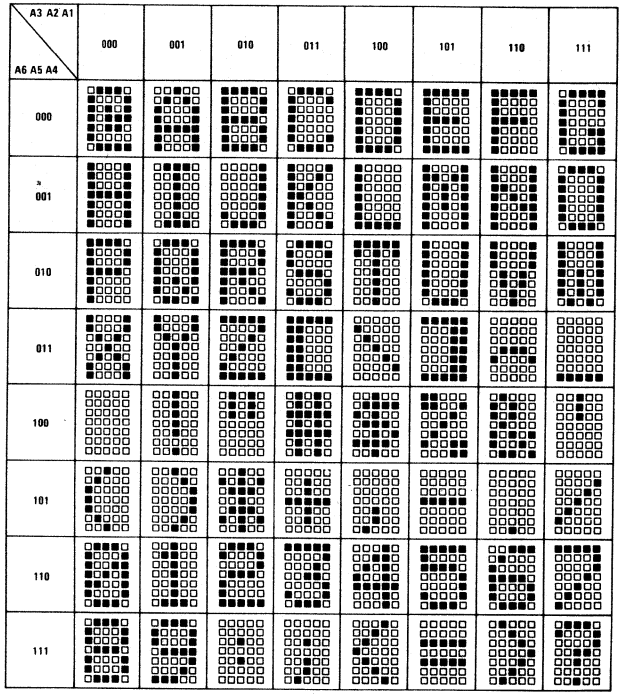
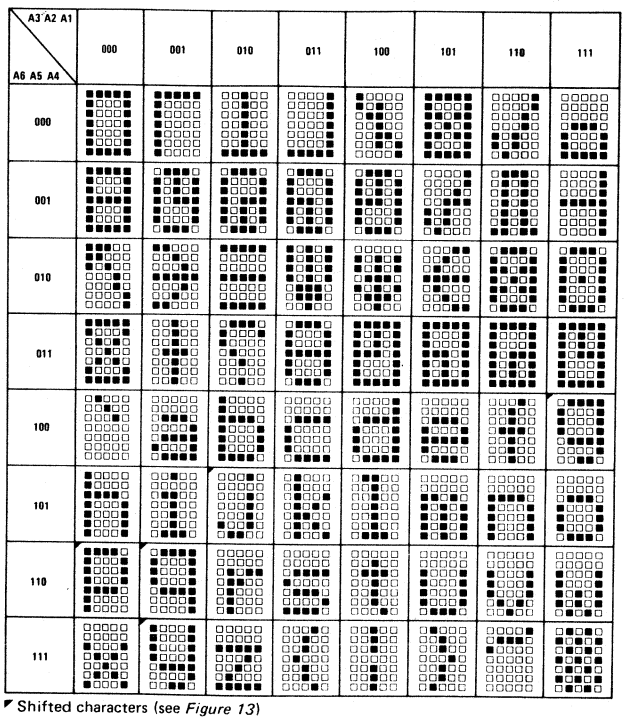


FIGURE 7. DM8767CAB



◤ Shifted characters (see *Figure 13*)

FIGURE 8. DM8678CAH

functional description (Continued)

Kata Kana Font will be Available in October 1977

FIGURE 9. DM8678CAD

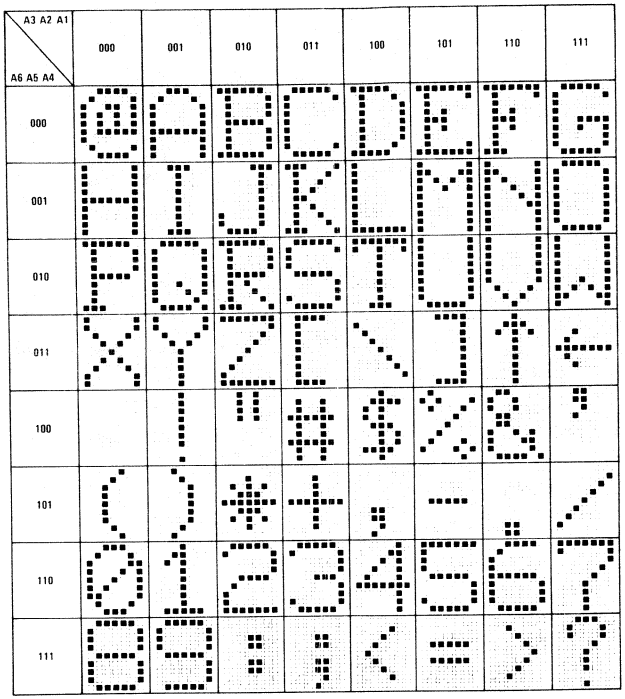


FIGURE 10. DM8678BTK

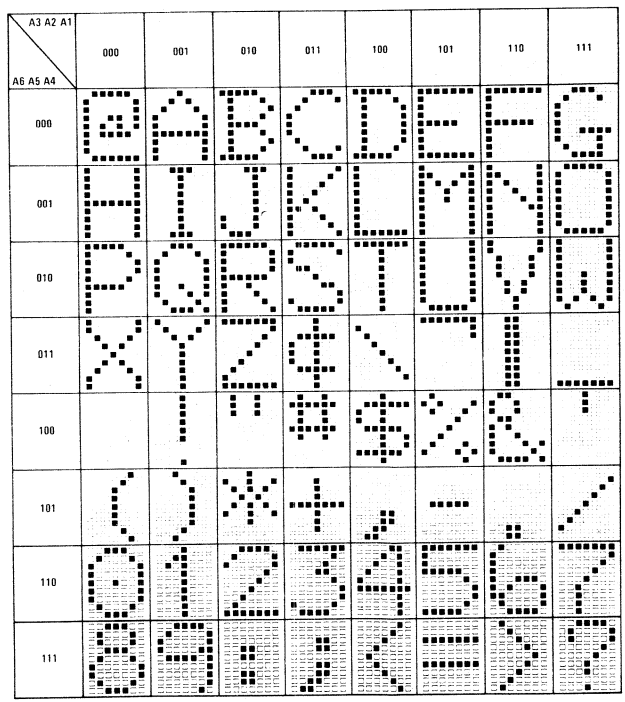


FIGURE 11. DM8678CAS

functional description (Continued)

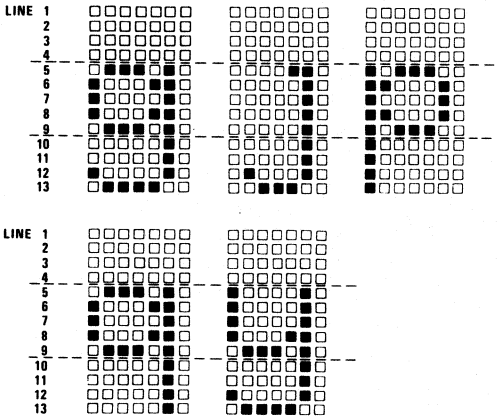


FIGURE 12. Shifted Characters for CAE

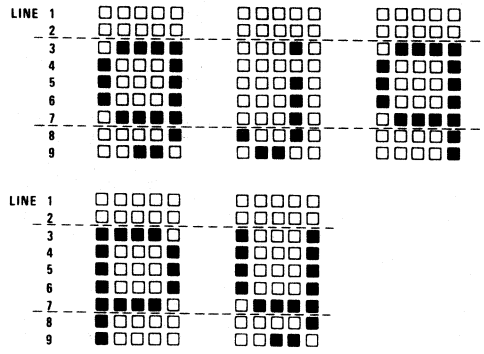


FIGURE 13. Shifted Characters for CAH

ordering information (For special character font for device DM8678).

CUSTOMER CARD INPUT FORMAT

Column 1–3
2-digit character address, from 0–63 preceded by a letter "C".

Column 4
Blank

Column 5–6
1-digit line address, from 0–8, preceded by a letter "L".

Column 7
Blank

Column 8–14
Row data which represents one horizontal row of dots at the specified line address and character address, with first dot at Column 8 and seventh dot at Column 14. Character for TTL high level is 1, for low level is 0.

Column 15
Blank

Column 16
Tag bit–0 for normal character and 1 for shifted character only.

Column 17
Blank

Column 18
Row SUM–Total number of "1's" presents in row data and tag bit expressed in decimal.

"TB" CARD FORMAT (total of eight cards)

Immediately following the data cards, there should be "TB" cards to indicate the column sum.

Column 1–2
The character "TB".

Column 3
1-digit corresponding to Dot number. Use number 8 for tag bit.

Column 4
Blank

Column 5–7
Column SUM–Total number of "1's" in column expressed in decimal.

truth table input format

CHARACTER ADDRESS	LINE ADDRESS	DOT DATA D1, D2, D3, D4, D5, D6, D7	TAG BIT	SUM
0	0			
0	1			
0	2			
0	3			
0	4			
0	5			
0	6			
0	7			
0	8			
1	0			
1	1			
1	2			
1	3			
1	4			
1	5			
1	6			
1	7			
1	8			
2	0			
2	1			
2	2			
2	3			
2	4			
2	5			
2	6			
2	7			
2	8			
.	.			
.	.			
.	.			
.	.			
. TB				

DM8678 BIPOLAR CHARACTER GENERATOR

The DM8678 is a 64 character bipolar character generator with serial output, and packaged in a standard 16-pin DIP designed primarily for the CRT display marketplace. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing, and character line spacing which are normally done with extra packages. *Figure 1* is a block diagram of the DM8678.

Address Latch

The address latches are "Fall Through" or "Feed Through" latches. The address latches are illustrated in *Figure 2*. When the address latch control signal is high, the character addresses "Fall Through" the latch. And when the address latch control signal goes low, the character addresses are latched. A 40 ns address set-up time is required.

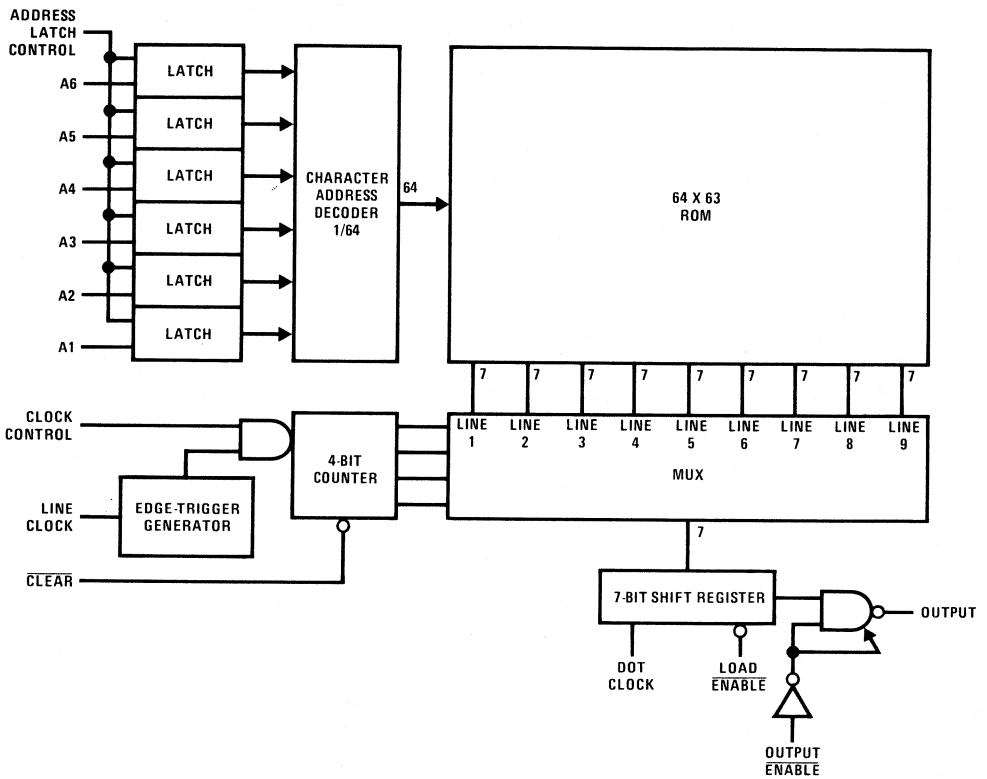
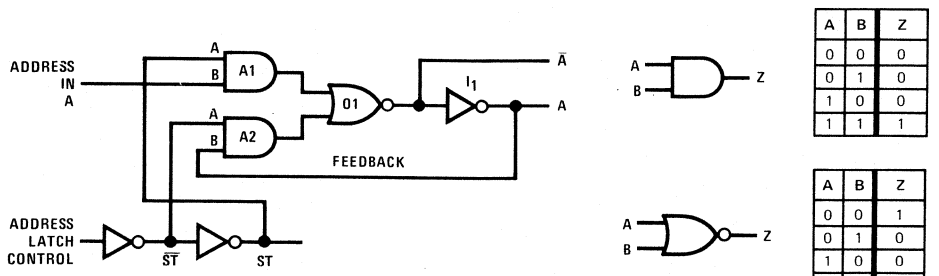


FIGURE 1. Block Diagram



A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

FIGURE 2. Address Latch

Logic operation is as follows: When the address latch control signal is high, "AND" Gate A1 is enabled and "AND" gate A2 is disabled. In this mode, data "falls through" the latch. When the address latches control signal goes low, Gate A1 is disabled, blocking any new address inputs. Gate A2 is enabled by a high on input "A" which allows the feedback to determine the output of gate A2. If the feedback is low, the output of A2 will be low. If the feedback is high, the output of gate A2 will be high. Note that there are two inversions from the output of gate A2 (O1 and I_1) to the feedback loop. Thus the feedback maintains the level that was present on inverter I_1 when the address latch control goes low.

ROM

The ROM is 64 x 7 x 9 = 4032 bits. The ROM comes with a standard upper case character set. And, it is possible to have custom fonts. A coding sheet is included with the data sheet. Obviously it is possible to make smaller characters by not using all of the ROM. For example, a 5 x 7 character set could be made. Also, it is possible to use two chips to obtain a larger character set.

Line Counter

The line counter consists of a 4-bit ripple counter with an asynchronous $\overline{\text{clear}}$ input. The input clock is shaped by an edge-triggered clock generator. The clock generator's output clock pulse is enabled by the clock control signal. The output pulse from the clock generator goes to one input of a two input "AND" gate and the clock control signal goes to the other input of the "AND" gate. When the clock control signal is low the clock pulse is blocked by the "AND" gate. The line counter is illustrated in *Figure 3*.

The line counter is a mod 16 counter and its count can be shortened by $\overline{\text{clear}}$, which resets the counter to its first state, when it goes to low state.

7-Bit Shift Register

A 7-bit parallel-in serial-out shift register is used to serialize the output data. Seven "D" flip-flops and seven 2-line-to-1-line multiplexers are used to perform the parallel to serial conversion. *(Figure 4)*

Operation of the parallel to serial converter is as follows: the cycle begins with load $\overline{\text{enable}}$ going low. This routes data from the ROM via the MUX to the "D" inputs of the 7 flip-flops. The data at the "D" inputs is clocked into the flip-flops on the next low-to-high transition of the dot clock. Next, the load $\overline{\text{enable}}$, goes high switching the mux. Now data at the "D" input comes from the "Q" output of the preceding flip-flop stage.

The first stage in the shift register is an exception and the mux routes a low to its "D" input, with the first stages "D" input low. After 7 clocks, all stages are low and any additional clocks will produce a low output. This feature is used for horizontal spacing between characters.

Output Buffer

The output buffer is a standard TTL TRI-STATE® output circuit. The $\overline{\text{output enable}}$ is the TRI-STATE control and when the $\overline{\text{enable}}$ is high, the output is in the Hi-Z state. The output can sink 16 mA at 0.45V for a low signal out, and, will source 2 mA at 2.4V for a high signal out.

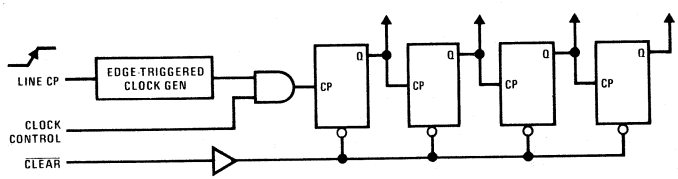


FIGURE 3. Line Counter

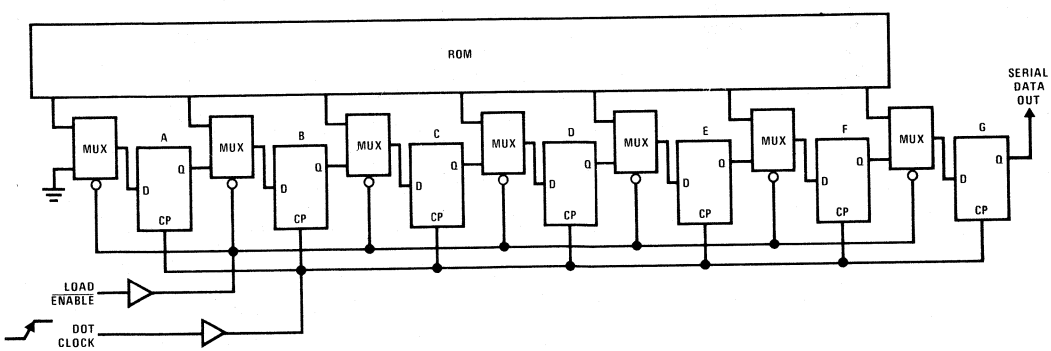


FIGURE 4. 7-Bit Parallel-In Serial-Out Shift Register with Synchronous Load

OPERATION OF THE DM8678 CHARACTER GENERATOR

To illustrate operation of the DM8678, an example is given tracing the sequence of events involved in generating a character. The character "N" is used in this example. *(Figures 1 and 5)*.

Generation of the character "N" begins with the appropriate 6-bit character address becoming valid on the address inputs A1 to A6. This address can be latched by bringing the address latch control signal low. There are address set-up and hold times of 50 ns and 40 ns respectively.

The output of the address latch is decoded in the character address decoder. This is a 1/64 active high decoder. The word line which contains the code would go high.

The ROM contains the code required for generating the 64 7 x 9 characters. The ROM is organized 64 words each, 63 bits long (7 x 9 = 63). In the ROM, the first 7 bits of 63 are line 1 of the character, the next 7 bits store line 2 of the character and so on. Note that 1 bit = 1 dot. The lines and dots for our example "N" are illustrated in *Figure 5*. The code for "N" would be:

1000001	1000001	1100001	-----
Line 1	Line 2	Line 3	
1000011	1000001	1000001	
Line 7	Line 8	Line 9	

After the access time has elapsed (tasl = 350 ns), the output of the ROM for Line 1 of the character (N for this example) can be loaded into the shift register. When load enable is brought low, the shift register is loaded on the next low-to-high transition of the dot clock with Line 1 of the character "N." The next 6 dot clocks will shift out the rest of the first line of character "N," If only a single character in a row was generated, the line clock would go from low-to-high advancing the line counter which in turn switches the multiplexer to Line 2 of the character. Line 2 contains the next 7 bits required for generating "N." This would continue until the 9th line has been clocked out. Any additional line clocks will put a vertical space between characters. This is illustrated in *Figure 5*.

In a typical application, more than one character is displayed in a row. *(Figure 6)* The sequence is as follows: Line 1 of the first character is clocked out. Note that 7 dot clocks are required to shift out one line in a character. Additional dot clocks will add lows to the end of the line. This provides a horizontal space between characters. There is no limit to the number of clocks which can be used to generate horizontal spacing. The address is changed to select the second character. Then the first line of the second character is clocked out, next, the first line of the third character is clocked out, continuing until the first line of the last character in the row has been clocked out. At this time, the line counter of the DM8678 is clocked, advancing the line counter to Line 2. The first character is addressed again, and the process of the scanning continues until the 9th line of the last character in the first row has been shifted out.

Then the line clock is again clocked, incrementing the line counter to Line 10. All characters in the row are scanned. *(Figure 6)* The output of the character generator for lines 10 to 16 is all lows. This provides a vertical space between rows. The number of lines used to space can be controlled by $\overline{\text{clear}}$ going low after the desired number of lines of vertical space have been generated.

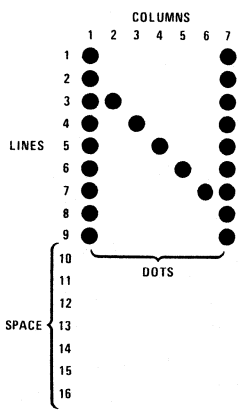


FIGURE 5. Character Example

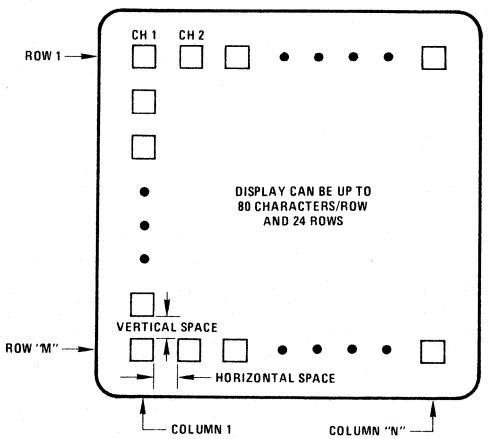


FIGURE 6. Display Example

Next, the first line of the first character of the second row is addressed and scanned. This continues until the 9th line plus lines for vertical spacing of the last character in the last row has been scanned. At this time the display field has been written. For a CRT Display, it is necessary to refresh the display. Displays are typically refreshed 30 to 60 times each second. Memory is required to store the character address so that they may be called up when required for refresh.

Figure 7 is the connection diagram and logic symbol.

DEFINITIONS

A1–A6: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if $\overline{\text{load}}$ is low or shifts data if $\overline{\text{load}}$ is high.

Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

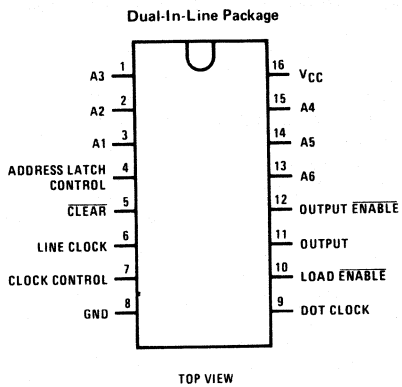


FIGURE 7(a). Connection Diagram

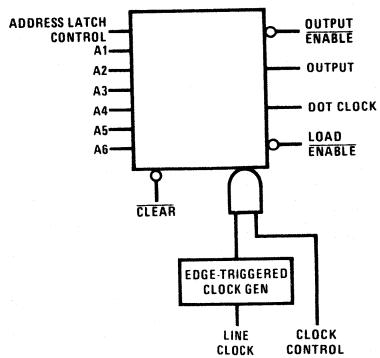


FIGURE 7(b). Logic Symbol DM8678

National Semiconductor

App Notes/Briefs

PROM Power-Down Circuits

description

Inexpensive bipolar PROMs can be used in high performance, low power applications if powered down when they are not being accessed. Since the access time of the circuit of Figure 1 is less than 80 nanoseconds, the power saving can be greater than 10 to 1 if cycled every microsecond. Longer cycle times, or decoding of the power switching to multiple packages, can yield even more impressive ratios.

Bipolar PROMs with on-chip power-down have power-up to power-down ratios of 3:1. Using the PROM power-down technique illustrated in Figure 1, ratios considerably higher than 3:1 can be obtained. National's PROMs perform well in this application. With power removed, the Tri-State® parts revert quickly to the third (open high Z) state. Because there are no clamp diodes from the outputs to V_{CC}, the powered down device presents only leakage to the output bus.

PROMs do not need to be continuously powered in many applications. Often data is required from a PROM on system power up or for a small percentage of a system cycle. Turning the PROM off when it is not needed saves power and the access time is increased by only the delay of the power down circuit.

The basic power down circuit is illustrated in Figure 2. A TTL level input signal drives the TTL logic input of the power down circuit. The logic input is drawn as a noninverting buffer; however, circuit operation is not limited to noninverting buffers. Logic Table 1 illustrates several logic implementations of both inverting and noninverting inputs with different speed-power tradeoffs.

Circuit operation is as follows. When the logic input to R_2 goes low, base drive is supplied to the PNP switch, turning the switch on. C_1 is a speed-up capacitor which decreases the switching time of the PNP switch. In applications where high speed is not important C_1 is not necessary. When the PNP saturating switch is on V_{CC} (+5 V) is applied to the PROM. The time delay from power up command to power up on the PROM ranges from about 10 ns to 100 ns, depending upon the PNP switch and the TTL logic driving the switch.

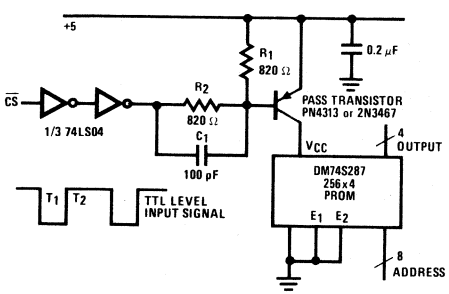


Figure 1. PROM Power Down Circuit

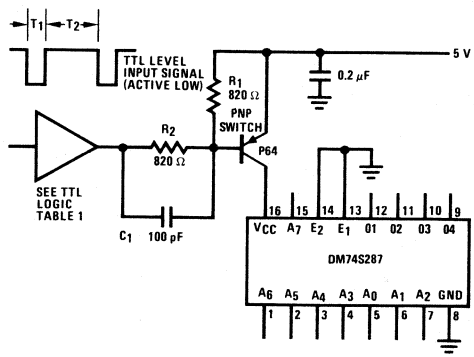


Figure 2. PROM Power Down Circuit

logic table

TTL LOGIC	
CS — 74S00 74LS00	• Fast • Active High Selects 74S00 Speed 74LS00 Speed and Low Power
$\overline{CS}$ — 74S04 74LS04	• Fast • Active Low Selects 74S04 Speed Only 74LS04 Speed and Low Power
$\overline{CS}$ — MM74C902	• Very Low Power • Active Low Selects Buffers can be connected in parallel for additional current
1/10 DECODER (4, 10) — MM74C42	• Very Low Power • Memory Expansion • No Resistors Required R_1 and R_2, Figure 2, not required

design example

Design a minimum power memory that has a 200 ns access time, a 1000 ns cycle time, and a 256x8 memory.

Two DM74S287 PROMs will be used for the 256x8 memory. DM74S287s have a ±5% power supply tolerance. Since there will be about a 0.2 V drop across the PNP switch we need to ensure that the V_{CC} requirement of the PROM is met.

Since speed is not of prime importance in this application we will select "slow" low power parts in the power down circuit. The 74C902 noninverting buffer will be used as the logic input device. This device is selected for its low power. 2N3467 PNP switch will be used as the pass transistor.

From the data sheets:

2N3467 PNP Saturating Switch

$V_{CE(SAT)}$	I_C = 150 mA	typ = 0.165	max	= 0.3
h_{fe}	I_C = 150 mA	typ = 120	min	= 40
$V_{BE(SAT)}$	I_C = 150 mA	typ = 0.8	max	= 1 V

DM74S287 PROM

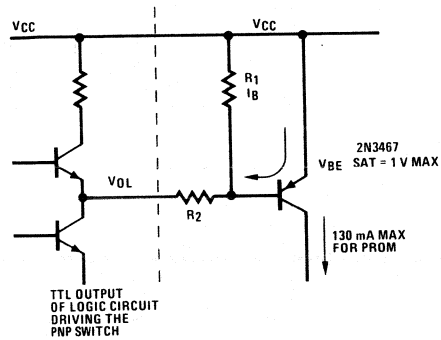
I_{CC} = 80 mA typ, 130 mA max

74C902 Buffer

I_{CC} = 15 μA max

We are now ready to calculate the value of resistor R_2. Resistor R_2 is used to limit the base drive current of the PNP 2N3467 transistor. The value of R_2 is calculated from the voltage across R_2 and the base current required to supply the I_{CC} current required for the PROM.

Resistor calculation:



$$I_B = \frac{130\text{ mA} = I_{CC}}{h_{fe} = 40} = 3.25\text{ mA}$$

min

Base current calculation:

$$R_2 = \frac{V_{CC} - (V_{BE(SAT)} + V_{OL(MAX)})}{I_B + \frac{V_{BE(SAT)}}{R_1 = 820}}$$

$$R_2 = \frac{5 - (1 + 0.5)\text{ V}}{(3.25 + 1.0)\text{ mA}}$$

$$R_2 = \frac{3.5\text{ V}}{4.25\text{ mA}} = 823\ \Omega$$

R_2 = 820 Ω, rounding to the nearest standard value.

R_1 is chosen to be equal to the R_2 to simplify the parts list and this allows resistor packs (8 identical resistors in a 16-pin package) to be used when appropriate.

Figure 3A is the final circuit for the 256 x 8 memory.

Performance of the 256x8 power down memory is:

Power when selected 1345 mW max

Power when deselected 0 mW with 74C902 buffer

Access time 180 ns max

Average power is a function of duty cycle, and for our 256x8 power down example average power is:

$$P_{ave(max)} = \frac{\text{on time}}{\text{off time}}.\quad \text{Power max} = \frac{200\text{ ns}}{1000\text{ ns}}.\ (665)\ (2)$$

$$P_{ave(max)} = \frac{1}{5}(1330) = 265\text{ mW max}$$

The 265 mW assumes that all parts are maximum at the same time. The more likely situation is that parts will be at or near their typical value.

For our example:

$$P_{ave(typ)} = \frac{1}{5}(830) = 166\text{ mW ave}_{typ}$$

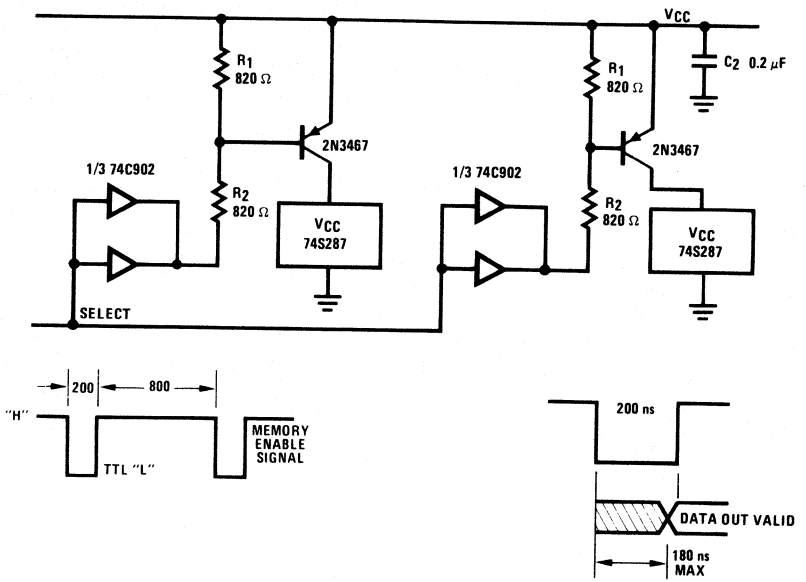
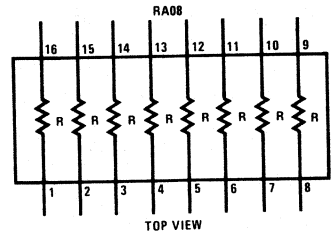


Figure 3A. 256x8 Power Down Memory

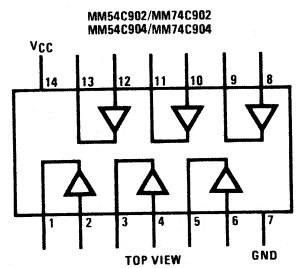
performance table

	Typ	Max
Access Time Max		
74C902 Buffer	54 ns	90 ns
2N3467 PNP Switch	20 ns	40 ns
74S287 PROM	35 ns	50 ns
	109 ns	180 ns
Power Selected		
I_B 2N3467		15 mW
74C902		— —
74S287 at 5 V, 6.65 mW each		1330 mW
		1345 mW
Power Unselected		
I_B 2N3467		0 (leakage)
74C902		0 (75 μW)
74S287		0
		0 mW

resistor



buffer



128 Characters with the DM8678

National Semiconductor
Memory Brief 1
W. Johnston
C. Mitchell
July 1977

The purpose of this brief is to describe the control logic necessary to generate 128 characters and attributes. The example used is for the upper and lower case set of characters from the DM8678BWF and DM8678CAE with cursor (underline) and blanking.

There are 2 important factors to consider when using 2 DM8678's. First, the character set of each ROM pattern is based on a 6-bit ASCII format. A seventh bit must be added for selection of upper or lower case. Second, the standard ASCII format requires that bits 6 and 7 be exclusive-ORed to select upper and lower case characters. Pipelining this altered most significant bit (bit 6 and bit 7) synchronizes the signal to control the OUTPUT ENABLE of the appropriate character generator. This either enables or TRI-STATES® the DM8678 outputs. *Figure 1* shows an implementation using the DM7486—exclusive-OR gate and the DM8511—gated D flip-flop.

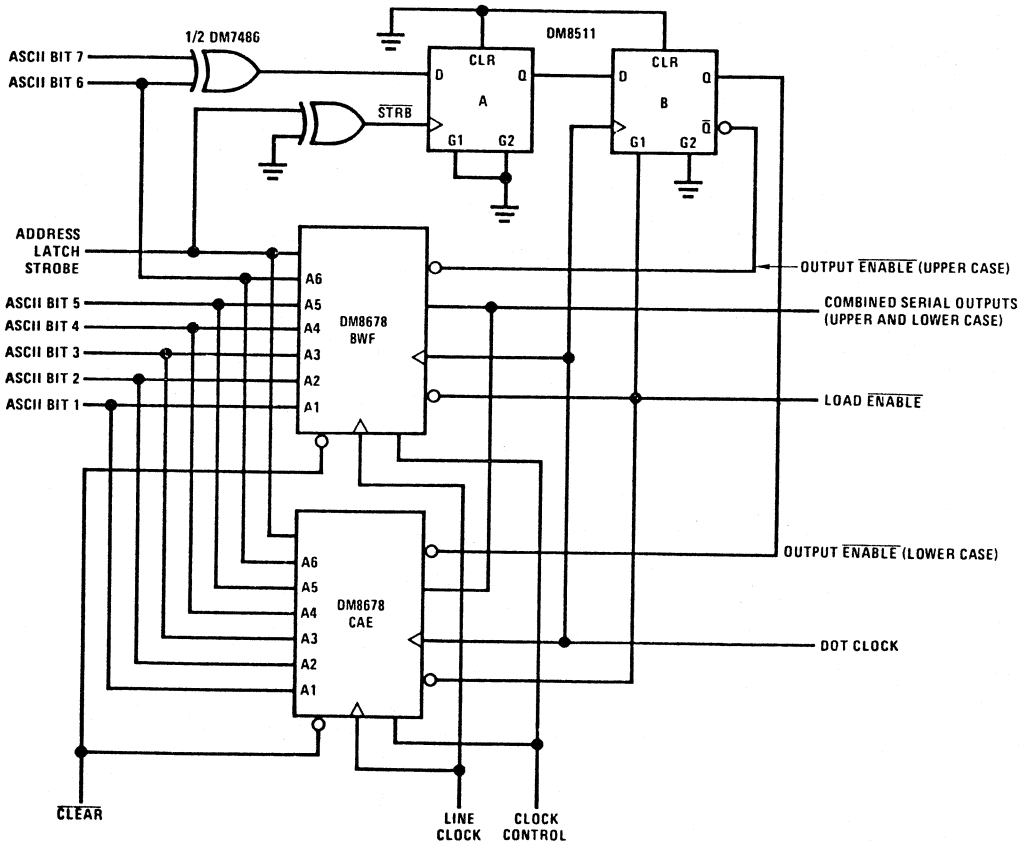


FIGURE 1. Upper and Lower Case Character Generator

The selection bit is latched into the first flip-flop on the trailing edge of the address latch strobe. If the strobe of the DM8678 is not in use (as in low character rate systems), then this first flip-flop (A) may be eliminated. The second flip-flop (B) is gated on by the same signal that drives LOAD $\overline{\text{ENABLE}}$ on the character generator. Clocking of both the DM8678's and flip-flop (B) occurs on the positive edge of the dot clock. Q and $\overline{\text{Q}}$ drive the OUTPUT $\overline{\text{ENABLE}}$ inputs of the lower and upper case generators, respectively.

Figure 2 indicates how attribute bits can be inserted into the combined serial output of *Figure 1* to produce character blanking or underlining. Here the attribute bits are pipelined using DM8511's and DM7474's.

In *Figure 2*, a cursor (which occurs on the video display as an underline) is gated on only during the eleventh scan line of a character. Apart from this gating the attributes are pipelined in the same manner as the OUTPUT $\overline{\text{ENABLE}}$'s in *Figure 1*, except that the outputs of the DM8511's are logically combined with the video.

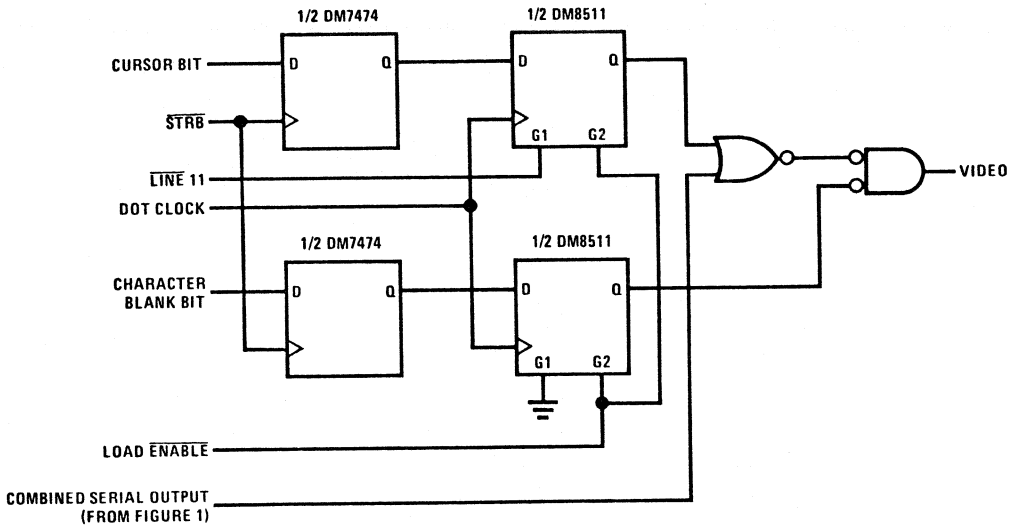


FIGURE 2. Pipelining Attribute Bits

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571610, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248

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4. RELIABILITY REPORTS

National Semiconductor

TITANIUM-TUNGSTEN SCHOTTKY BIPOLAR PROMS

Preliminary Issue
August 1977

Abstract

National's Reliability Assurance Department maintains an active program of product reliability evaluation on all products and processes.

This report summarizes the work specifically undertaken on the Schottky Bipolar 1024-bit PROM utilizing titanium-tungsten (Ti-W) fuses in Epoxy B molded dip (N-package), cerdip (J-package), and hermetic dip (D-package).

To date, in excess of 1000 devices have been subjected to various accelerated tests including dynamic high temperature operation life, temperature-humidity life, temperature cycling and thermal shock. Device performance in all package configurations is excellent.

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PRODUCT DESCRIPTION

National's DM74S287 TRI-STATE® 1024-bit PROM and DM74S387 the open collector version, are the first of a series of Schottky Bipolar field programmable memory products utilizing titanium-tungsten fuse technology. 2048-bit and 4096-bit devices are currently under evaluation and will be discussed in detail in later issues of this report.

The use of titanium-tungsten (Ti-W) as a 'buffer' material between the aluminum interconnect and the platinum-silicide 'barrier' is a standard of the Schottky Bipolar process metalization system. (Refer to Figure 1)

Utilizing titanium-tungsten as a fuse metal therefore 'uncomplicates' the metallic structure of these Bipolar PROMS.

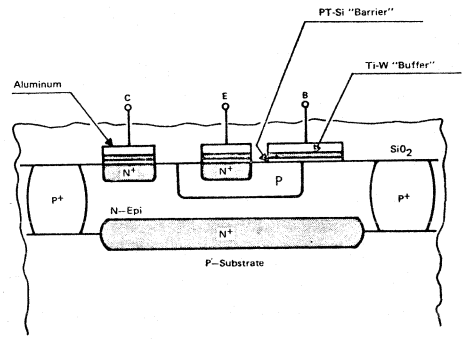
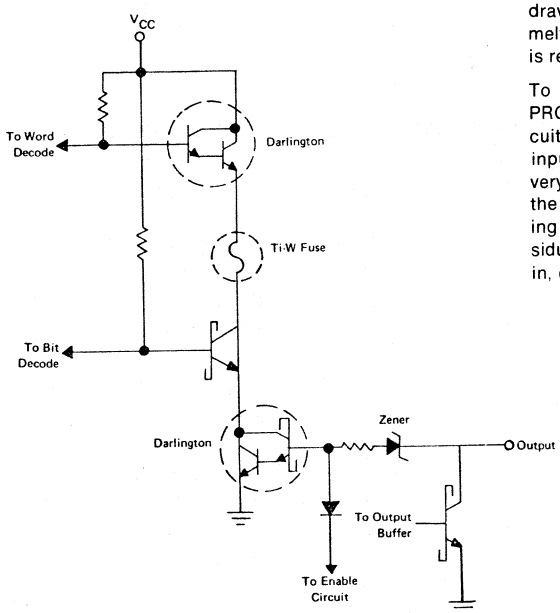


Figure 1

Titanium-tungsten has many desireable properties which make it a preferable fuse material. It is extremely stable metal which does not oxidize readily and is very 'processable'. Thus, fuses of uniform size (NOM: 2μ x IKÅ) and resistivity are readily produced. The one drawback of Ti-W as a fuse material is its extremely high melting temperature (3300 ° C). A very high energy pulse is required to open the fuse.

To insure reliable programming, National's Ti-W PROMS incorporate the Darlington programming circuit shown in Figure 2. This circuit 'pulse shapes' the input from the programmer and provides a high energy very fast current pulse to the selected fuse. Because of the speed of this on-the-chip approach localized heating is minimized. This results in a wide gap free of residual material, and as demonstrated by the data herein, excellent reliability.



TESTS PERFORMED

Accelerated testing methods are utilized by two operating groups within the Reliability Assurance Department to establish and monitor product reliability. These two groups are: Reliability Engineering, and the Reliability Audit Group. Data from both of those sources is included in this report.

The Engineering Group has the primary responsibility of evaluation and qualification of new or changed products and processes, while the Audit Groups responsibility is to periodically monitor product already qualified and released to production.

The tests utilized in the Reliability Audit program for molded products are as follows:

1. High temperature life test – TA = 125 °C, dynamic operation (refer to burn-in circuit 1305RE) 1000 hours.
2. Temperature/humidity life – TA = 85 °C/85% RH static bias, minimum power, 1000 hours.
3. Temperature cycling, 0 °C to 125 °C, 2000 cycles.

Tests included in the hermetic product audit program are:

1. High temperature life test – TA = 125 °C, dynamic operation (refer to burn-in circuit 1305RE), 1000 hours.
2. Thermal shock – 55 °C to 125 °C, 15 cycles, hermeticity fine leak and gross leak endpoints.
3. Solderability/MIL-STD-883A
4. Lead integrity/MIL-STD-883A.

The test methods utilized by Reliability Engineering are for the most part the same as those utilized in the audit program, however, temperature extremes and durations are often extended, applied voltages worst-cased, and step stress and mean life-time programs employed.

These two programs combined with field failure data fed back through our failure analysis organization provide National Reliability Assurance with excellent visibility into our product's reliability.

Note: All entries in this report are identified by file number. These reliability files are COMPANY PRIVATE, however, they can be made available for inplant review upon request.

TEST SAMPLE DESCRIPTION

The following data describes the samples subjected to Reliability Assurance evaluations on our current Ti-W Schottky Bipolar PROM process. (By date code).

FILE NO.	PART NO.	PACKAGE	DATE CODE	QTY.	TYPE OF EVALUATION
AMB-16152	DM74S287	N	7633	115	Audit
AMB-16187	DM74S287	N	7639	115	Audit
RMB-76214a	DM74S287	N	7647	28	Engineering Eval.
RMB-76214b	DM74S287	N	7647	33	Engineering Eval.
RMB-76214c	DM74S287	J	7648	14	Engineering Eval.
RBM-76219	DM74S287	J	7648	40	Engineering Eval.
AMB-17045	DM74S287	N	7702	115	Audit
RMB-77035	DM74S387	D	7707	27	Engineering Eval.
AMB-17096	DM74S287	N	7709	115	Audit
RMB-77038a	DM74S287	D	7709	90	Engineering Eval.
RMB-77038b	DM74S287	J	7709	60	Engineering Eval.
RMB-77038C	DM74S287	N	7709	90	Engineering Eval.
RMB-77039a	DM74S287	N	7709	150	Engineering Eval.
RMB-77039b	DM74S287	J	7709	90	Engineering Eval.

Note: All reliability tests are performed on partially programmed devices so that both programmed and unprogrammed fuses may be studied.

SEMICONDUCTOR DEVICE RELIABILITY & THE ARRHENIUS MODEL

Anyone who has dealt with the reliability problem will instantly recognize the curve of Figure A. This is the famous "bathtub" curve which plots failure rate against time. This idealized curve applies to all hardware – mechanical, electrical, or electronic. There are three vital statistics associated with this curve.

INFANT MORTALITY

These are the devices that fial during the early-life period from t_0 to t_1. This number is represented by the shaded area under the curve. Since the failure rate (λ) is decreasing rapidly during the early-life period, failure rate is a meaningless statistic during this period. Infant mortality is expressed as an absolute percentage. Generally speaking, the early-life period extends from a few weeks to a few months. The infant mortality is greatly influenced by system stress conditions other than temperature and can vary widely from one application to another with the same device.

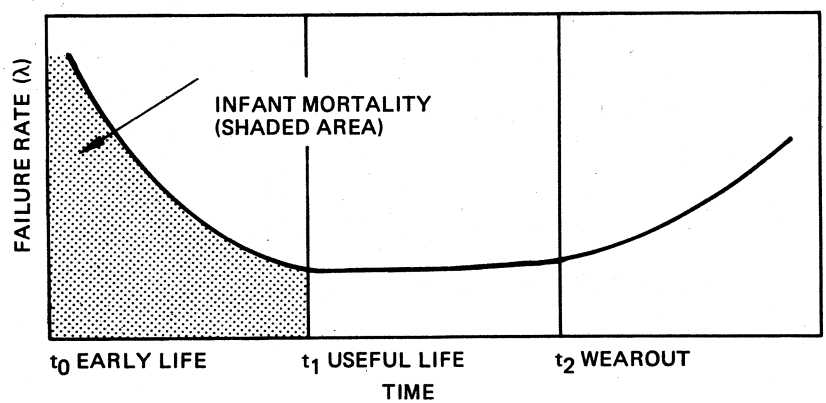
FAILURE RATE

The useful failure rate is the average failure rate that can be expected from a device population after the early life period has passed and before wearout failures begin. This is represented by the flat portion of the curve from t_1 to t_2. This statistic is usually expressed as percent failures per 1000 hours. Other units such as failures per million hours are also used. Another way of stating this statistic is mean-time-between-failures (MTBF). The MTBF is expressed in hours and is simply the reciprocal of the failure rate. The useful-lifetime period may be only a matter of a few months but it usually extends for decades if proper design margins are applied. The primary stress which influences the useful failure rate is temperature.

USEFUL LIFETIME

This is the period which extends from the end of early-life to the beginning of the wearout region. This is represented by the tail of the curve beyond t_2. At this point, true wearout failures begin to occur in significant numbers. This statistic is normally expressed in hours. In most cases, there is insufficient data available to define the true, useful lifetime of a device. However, a minimum useful lifetime figure will usually suffice as a basis for assuring adequate design margins. Temperature plays a major role in determining the onset of wearout mechanisms but other stresses such as pressure, mechanical stress, thermal cycling, and electrical load conditions play first-order roles as well.

FIGURE A
RELIABILITY LIFE CURVE



The only practical way to estimate failure rate and useful lifetime figures is through the use of accelerated life testing of sample guantities of devices which are known to represent the device "population". There are numerous accelerated life tests which can be performed on devices but the most common test is the high temperature operating life test. It is a well-established fact that the vast majority of long-term failure mechanisms (i. e. other than infant mortality mechanisms) are time and temperature dependant. Their frequency and distribution in time usually follows a log-normal distribution and the effect of temperature on this distribution can be predicted by the use of the Arrhenius Model. This model permits the estimation of failure rates at junction temperature conditions different from the junction temperature condition during an accelerated test. The Arrhenius Model was developed in the 1880's as the law which describes the reaction rates of chemical processes. Its adoption as an aid in solcing accelerated life testing problems came about because of very logical reasons. The researchers in the field of accelerated life testing methods experimented by performing tests and then attempted to explain these empirical results in physical terms. The need for a physical explanation of empirical results is of paramount importance in the complete validation of an accelerated life testing method. In many of the simple electronic parts, it is easy to theorize that the mechanisms leading to degradation and failure are chemical processes and elevated temperature is frequently selected as an accelerating stress. Hence it seemed a natural course of events to attempt to apply this as a useful adjunct to the state of the art of accelerated life testing. The Arrhenius Model as applied to accelerated life testing methodology assumes that the degradation of some performeter is linear with time with the rate of degradation depending on the severity of the

accelerating stress. It further assumes that the logarithm of the degradation rate varies linearly with the reciprocal of the absolute temperature. Therefore, the following formula is used to relate equivalent failure rate at accelerated stress levels to calculated failure rate at use stress levels.

TABLE I

COMMON WEAROUT FAILURE MECHANISMS

FAILURE MECHANISM	ACTIVATION ENERGY
Electromigration in aluminum conductors(glassed,largegrain)	1.2eV
Intermetallic growth in gold/aluminum bond systems	.99–1.04eV
Wire and wire bond failures during thermal cycling	A fatigue mechanism
Slow trapping–charge injection	1.0–1.3eV
Chargeaccumulation–mobileions	1.0–1.35eV

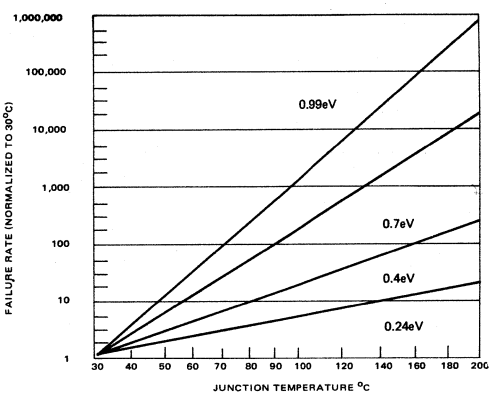


FIGURE B
FAILURE RATE AS A FUNCTION OF JUNCTION TEMPERATURE

Table I lists some of the more common long term failure mechanisms together with their activation energies. All of these mechanisms are discussed at length in the literature. They are essentially all wearout mechanisms. The dramatic acceleration effect of temperature on these failure mechanisms is illustrated in Figure B. This family of curves shows MTBF versus junction temperature for various of activation energy. As can be readily seen from these curves, a mechanism with an activation energy of .99eV is accelerated more than 800 times when the junction temperature is increased from 50 °C to 125 °C. This means that a 1000 hour life test at a junction temperature of 125 °C is the equivalent of 800,000 hours of device operation at a junction temperature of 50 °C. Assuming theat the 1000 hour test at 125 °C fails to reveal an increasing failure rate (i.e. onset of wearout), a 1000 hour test would substantiate a minimum useful lifetime in excess of 90 years.

At this point, we are faced with a dilemma. Since each failure mechanism has a unique activation energy it is obvious that there is no such thing as a "universal" acceleration curve which is good for all mechanisms under all conditions. Furthermore, treating each failure mechanism independently becomes a superhuman task best suited to the dedicated researcher with unlimited time and resources. One practical approach therefore would be to use the lowest known value of activation energy (consistent with common sense) so that all failure rate estimates are "pessimistic". This is the approach used in MIL-HDBK-217B. An activation energy of 0.7eV was used for the π_T factors applicable to Bipolar deviees. While the rationale for selecting this value of activation energy is not discussed in MIL-HDBK-217B, it would appear likely that the authors of this document has access to some fata which has not been heretofore published. However, for the sake of consistency, National basis its published estimated failure rate figures on the activation energy figures used in MIL-HDBK-217B.

$$t = t' \exp \frac{-E}{K} \left(\frac{1}{Tj'} - \frac{1}{TJ} \right)$$

Where: t = MTBF at junction temperature Tj

t' = MTBF at junction temperature Tj'

Tj = junction temperature in °K

E = thermal activation energy in electron volts (eV)

K = Boltzmann's constant (8.617×10^{-5} eV/°K)

DM74S287
LIFE TEST

DISTRIBUTION OF FAILURE DM74S287
LIFE TEST HOURS
(TA = 125 °C)

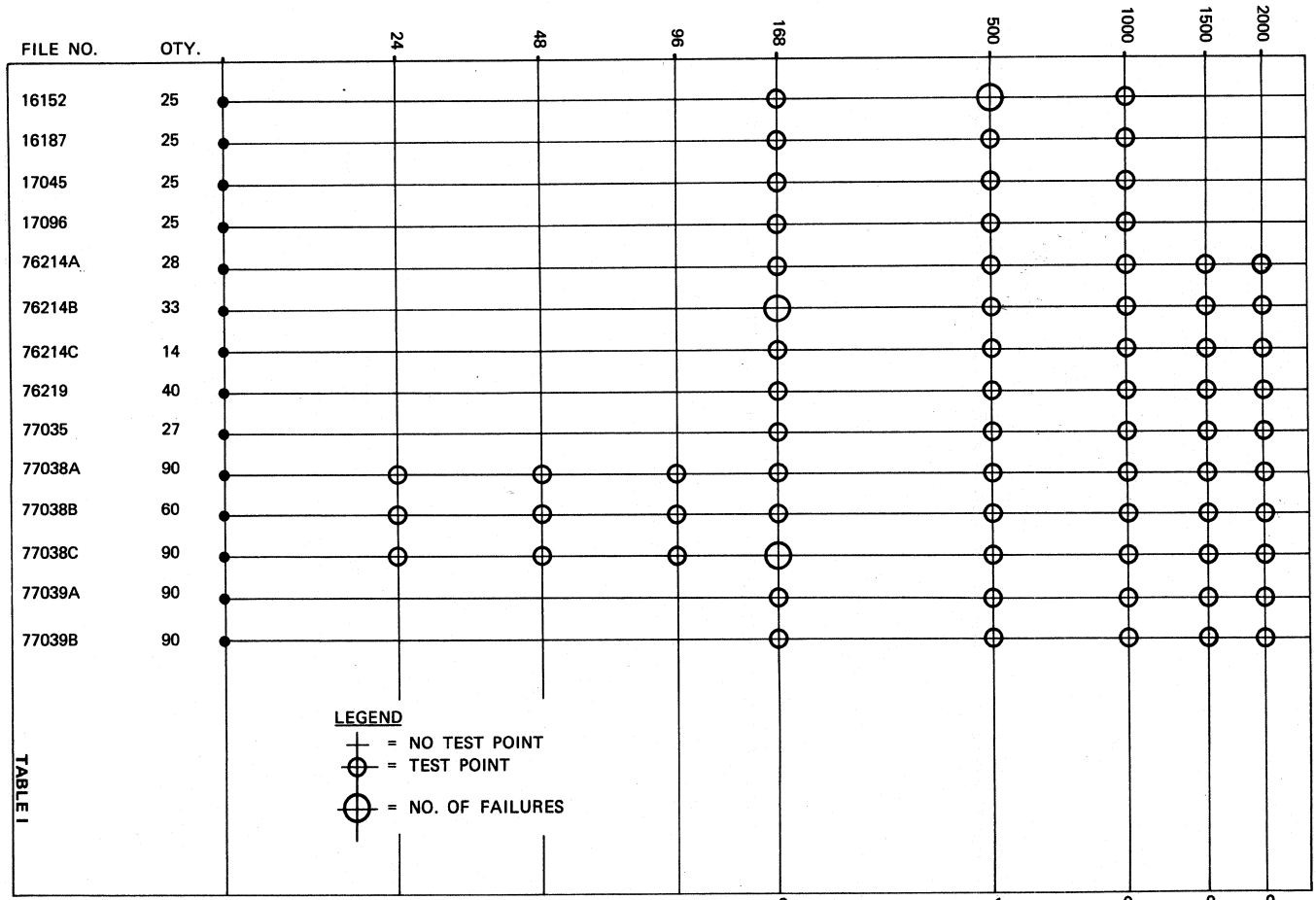


TABLE I

TOTAL # FAILURES = 3
TOTAL DEVICE HOURS = 1,131,636

LIFE TEST RESULTS

As can be observed in Table I, to dare only three failures have occurred as a result of high temperature accelerated life testing. Analysis of these failures has indicated the following:

TEST	ANALYSIS
AMB-16152 STATIC BIAS, HIGH TEMPERATURE LIFE TEST. 1 Failure © 504 hrs.	FUNCTIONAL FAILURE, LOW BREAKDOWN E2 INPUT GATE, OXIDE DEFECT
RMB-76214B DYNAMIC OPERATION, HIGH TEMPERATURE LIFE TEST S/N 06 FAILURE © 168 hrs.	PARAMETRIC FAILURE OUTPUT 04 LEAKAGE EXCEEDS SPECIFICATION JUNCTION LEAKAGE
RMB-77038C DYNAMIC OPERATION, HIGH TEMPERATURE LIFE TEST S/N 01 FAILURE © 168 hrs.	FUNCTIONAL FAILURE MARGINAL ADDRESS ACCESS TIME. OXIDE LEAKAGE.

It is important to note that none of the failures observed during the first 1,000,000 device hours are fuse related, substantiating the excellent reliability of the titanium-tungsten system.

FAILURE RATE EXTRAPOLATION

Based on the failure data supplied herein, a more appropriate activation energy might be applied to calculate a failure rate for this product, however, because of the limited number of failures observed and to be compatible with MIL-HDBK-217B, an activation energy of 0.4e.v. is utilized in the following calculation:

TEST CONDITIONS

Vcc = NOMINAL 5,0 Volts
Icc = 75mA (Avg. [3] Temperature, 50% Duty Cycle)

PD = 375mw

ΘjA = 65 °C/Watt (Still Air) D or J package

ΘjA = 115 °C/Watt (Still Air) Molded Dip (N)

Air Flow = 300 Lin.Ft/Min (Approximately 75% of Still Air Value)

Tj (Test) for D or J package = Ambient + 18 °C

Tj (Test) for N package = Ambient + 32 °C

Life test data given includes all package types therefore, for the purpose of this calculation an average Tj of ambient + 25 °C is used.

TA = 125 °C + 25 °C = Tj' (Test) = 150 °C

ASSUMED USE CONDITIONS

Vcc = NOMINAL 5.0 volts

Icc = Typical 80mA

TA = 30 °C AIRFLOW 300 Lin. ft/Min.

Θj Averaged for above conditions
All package types = TA + 25 °C.

Tj (use) = 55 °C

Applying the Arrhenius relationship we find:

Tj' (Test) 150 + 273 = 423 °K
Tj (Use) 55 + 273 = 328 °K

$$\frac{0.4}{8.617164044 \times 10^{-5} \text{e.v./°K}} = 4641{,}89$$

$4641.89 \div {}_{e}Tj' - Tj = 24x$

Thus 1, 131, 636 = 2.72×10^{7} Equivalent hours.

$$\frac{3 \text{ Failures}}{2.72 \times 10^{7} \text{ hrs.}} = 0.0245\%/1000 \text{ hrs.}$$

at 90% confidence.

National Semiconductor

MM1702A ELECTRICALLY REPROGRAMMABLE ROM

CONTENTS

1.0 INTRODUCTION

This report has been written to furnish reliability information concerning National Semiconductor's MM1702AQ 2048-bit electrically programmable (UV erasable) read only memory (EPROM). The MM1702AQ is manufactured using National Semiconductor's proven P-channel Silicon-gate technology, utilizing the floating gate avalanche injection Metal-Oxide-Semiconductor (FAMOS) cell structure.

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2. Basic Cell Structure

As previously indicated, the basic FAMOS cell structure is fabricated using National Semiconductor' well-established P-channel Silicon gate process. Figure 1 shows the main physical features involved in the FAMOS structure.

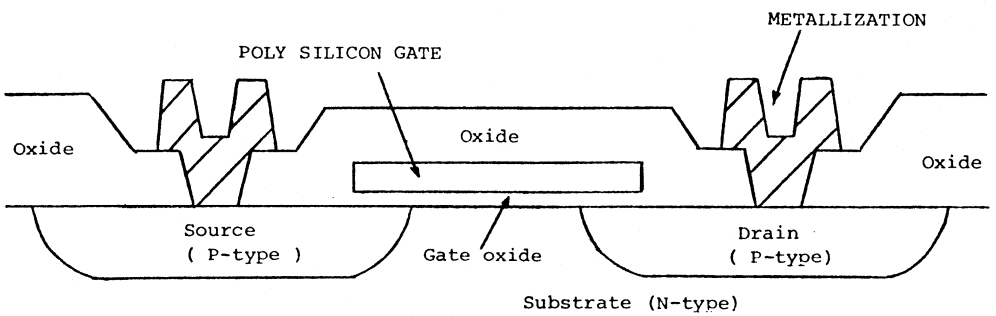


Figure 1 Physical Construction of Floating Gate

3. Mode of Operation

3.1 Programming

Figure 2 shows the cell structure under bias.

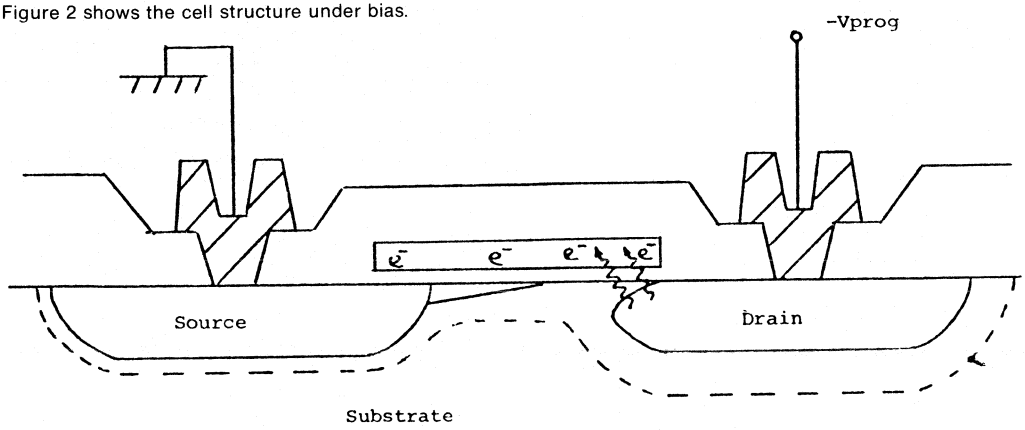


Figure 2 Floating Gate in Programming Mode.

On the application of a programming voltage, -Vprog, to the drain, avalanching occurs in the region of the gate/drain overlap and "hot electrons" are injected onto the gate. When sufficient charge is injected onto the gate, the substrate region between source and drain then becomes inverted. In this condition, the cell is programmed "ON" while the state of the cell is determined by sensing source-drain conductivity.

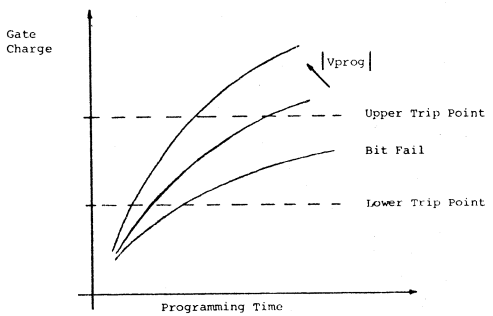


Figure 3 Floating Gate Charging Characteristics with Respect to Programming Voltage & Programming Time

The amount of charge injected onto the gate is a function of the magnitude and duration of the programming charge as indicated in Figure 3 above. Additionally, the time to charge each bit varies from address to address due to basic processing characteristics. Through characterization and reliability testing, the amount of charge required on the gate to guarantee operation and long term data retention has been established.

3.2 Erasure

The programmed "OFF" state exists when there is no charge on the floating gate. Gate discharge (erasure) is accomplished by illuminating the chip with short-wavelength (253,7nm) ultraviolet light at 6W-sec/cm^2. The previously injected electrons on the gate are energetically excited such that a photocurrent flows from the gate back to the drain. Now that the gate has been discharget, the substrate surface between source and drain is no longer inverted and the sense amplifier detects the conductivity change.

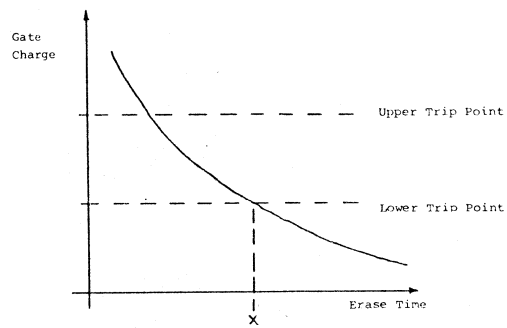


Figure 4 Charged floating gate characteristics with respect to erase time.

The actual time required for erase depends on such variables as the amount of charge stored, UV transmissivity of the quartz lid, distance from the source, etc. From the users point of view, the main variables of concern are distance from the source and the light source itself. It is recommended that the lamp be placed $^1/_2-1$ inch from the chip. Each lamp should be calibrated, a worse case erase time (X) established then overerase by a factor of two, as indicated in Figure 4 above.

4. Test Philosophy

4.1 Production Testing

In addition to ensuring all guaranteed parameters are met, each MM1702AQ cell undergoes programing and erase at least twice during its standard production test flow. Furthermore, before being given final approval, each unit is subjected to a high temperature screen bake at 225 °C, and retested in order to guarantee its data retention properties.

4.2 Box Stock Quality Audit

As a further quality monitor, routine sampling of Box Stock is carried out, both with respect to full data sheet specifications and data retention.

5. Reliability

Regular extended life testing of MM1702AQ's carried out by means of the following industry standard accelerated stresses:

(1) High temperature (+ 125 °C ambient) reverse bias (HTRB)
(2) Dynamic high temperature (+ 125 °C ambient) operating life (DHTL)
(3) High temperature (+ 125 °C ambient) data retention bake.

The combination of all three stress modes allows analysis of any failure mechanism evident in terms of process and/or product stability. It is required that continued satisfactory performance to the above accelerated life tests be the basis on which the production test flow and AQ monitors are justified.

5.1 High Temperature Reverse Bias (HTRB)

Figure 5 shows the DC biasing arrangement employed for an accelerating ambient temperature of + 125 °C.

Table 1 shows typical results obtained when units are subjected to HTRB. The data from Table 1 is again shown in summarized form in Table 2 to give the failure rates at 55 °C and 70 °C.

Sample Size	Device Hours	T_A(°C)	No. Fails
30	120,000	125	0
42	63,504	125	0
66	133,980	125	1
24	24,000	125	1

Table 1 HTRB Results

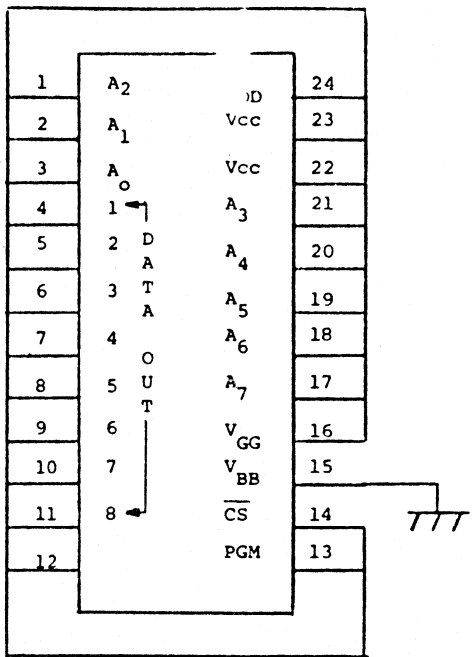
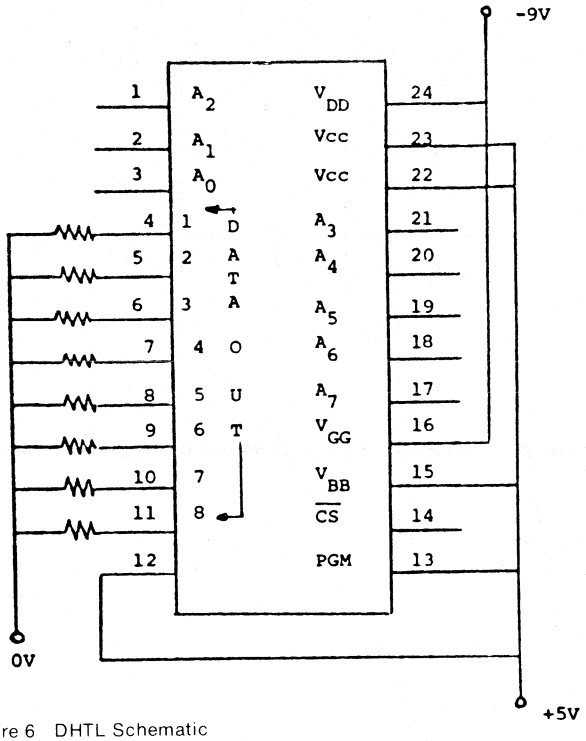


Figure 5

Total Device Hrs at 125 °C	Equivalent Device-Hours (0.7eV)	No. Fails	Failure Rate (%/1000 Hrs) at 60% Upper Confidence Level	Failure Rate (%/1000 Hrs) at 90% Upper Confidence Level
341,848	4.44×10^7 (55 °C)	1	0.005	0.009
	8.54×10^6 (70 °C)	1	0.025	0.048

Table 2 HTRB Failure Rate Calculations



Resistors: all 10kΩ, 1/4W

Addresses:

50% duty cycle, 0 to +5V

timings:

A_0 - 5μS
A_1 - 10μS
A_2 - 20μS
A_3 - 80μS
A_4 - 160μS
A_5 - 360μS
A_6 - 720μS
A_7 - 1440μS
$\overline{CS}$

Figure 6 DHTL Schematic

Figure 6 shows the operating conditions under which dynamic stress is carried out at the accelerating temperature of + 125 °C ambient. Typical data obtained is shown in Table 3 and in summarized form in Table 4 to give failure rates at 55 °C and 70 °C.

Sample Size	Device Hours	T_A(°C)	No. Fails
23	46,690	125	0
179	363,370	125	1
20	40,600	125	0

Table 3 DHTL Data

Total Device Hrs at 125 °C	Equivalent Failure Rate (%/1000 Hrs) Device-Hours (0.7eV)	No. Fails	© 60% Upper Confidence Level	© 90% Upper Confidence Level
450,660	5.9×10^7 (55 °C)	1	0.0036	0.0065
	1.1×10^7 (70 °C)	1	0.02	0.04

Table 4 DHTL Failure Rates

5.3 Data Retention

In this test, units are stored programmed at high temperature (225 °C) to accelerate charge leakage from the floation gates. Characterization of the leakage rates (Figure 6) at various storage temperatures shows two mechanisms causing charge decay. The data in Figure 7 has been re-plotted in Figure 8 to more clearly show the existence of the two different activation energies for the lower and opper portions of Figure 7 (indicated as A & B respectively). As shown, these curves correspond to activation energies of 0.7eV and 1.5eV, characteristic of surface state trapping (Qss) & ionic drift (Q_{NA}) respectively.

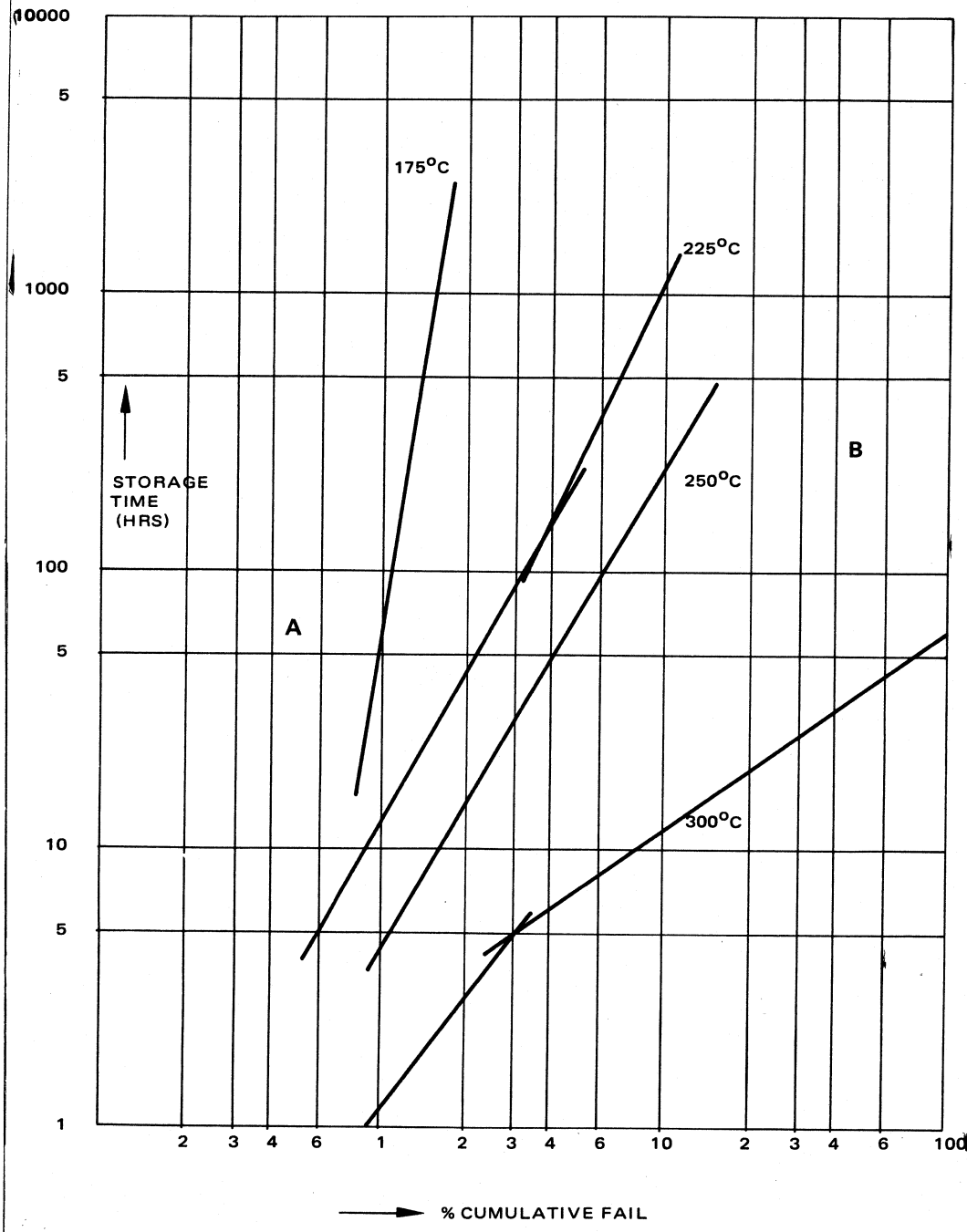


Figure 7 Data Retention Characteristics with Bake Temperature

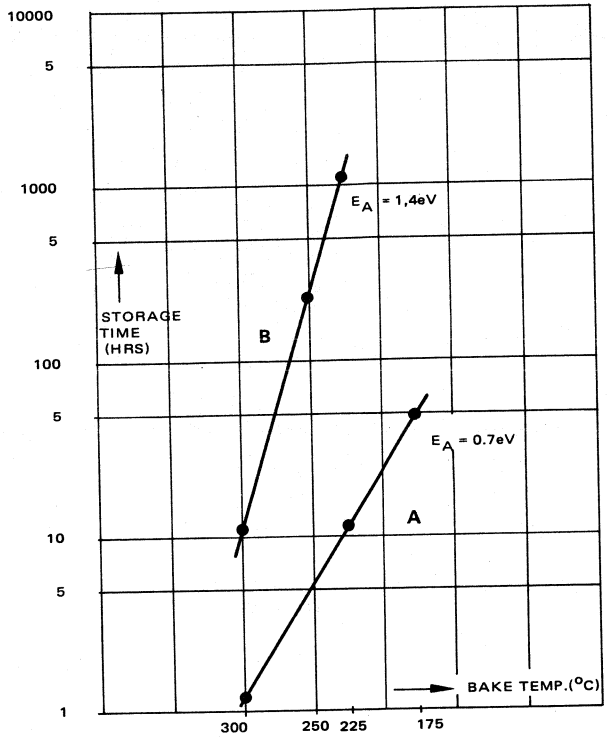


Figure 8

From the users point of view, data retention performance on the lower portion of the curves is of particular importance as representing worst case data retention lifetime. The data on the lower portion of the 225 °C Storage temperature is shown in Table 5 and the resultant calculated failure rate is given in Table 6.

Sample Size	Device Hours	T_A(°C)	No. Fails
255	35,178	225	9

Table 5 Worst Case Data Retention Fail Data at 225 °C Storage

As is evident from Table 6, the worst case failure rate for data retention is those for dynamic and static operation.

5.4 Packaging

A further routine monitor that MM1702AQ's undergo is cycled thermo-mechanical stressing to determine hermeticity lifetime of the quartz lidded ceramic package. Again industry standard tehcniques are employed consisting of:

(1) −65 °C to +150 °C, air-air & liquid-liquid
(2) −55 °C to +125 °C, air-air-, & liquid-liquid
(3) 0 °C to +125 °C, air-air.

In each of the above cases, typically, no failures are observed for 3,500 unit cycles.

Total Device Hrs at 225 °C	Equivalent Device-Hours (0,7eV)	No. Fails	Failure Rate (%/1000 Hrs) at 60% Upper Confidence Level	Failure Rate (%/1000 Hrs) at 90% Upper Confidence Level
35,178	$4{,}38 \times 10^8$ (55 °C)	9	0,003	0,004
	$8{,}75 \times 10^7$ (70 °C)	9	0,013	0,018

Table 6 Worst Case Data Retention Falure Rate

National Semiconductor

RELIABILITY REPORT
(PRELIMINARY)
MM2708
8K UV ERASABLE
PROM

August 1977

CONTENTS

1. INTRODUCTION

The 'High Performance 8192-bit Erasable PROM' has been developed and currently manufactured at 'National' in response to the increasing requirements of second generation microprocessors. The design goals of density and speed have been achieved through the development of an N-channel stacked-gate cell concept combined with novel peripheral circuits. The small cell size and fast memory access extend this new 'EPROM' performance beyond the levels established by the well known P-channel approach.

This report furnishes the device description and the reliability information concerning National Semiconductor's MM2708Q, 8192-bit 'EPROM'.

Prepared by:

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Approved by:

R. A. Kramer
Manager, Reliability Assurance

2. DEVICE DESCRIPTION

National's 2708 is packaged in an industry standard 24-pin package as shown in Figure 1.

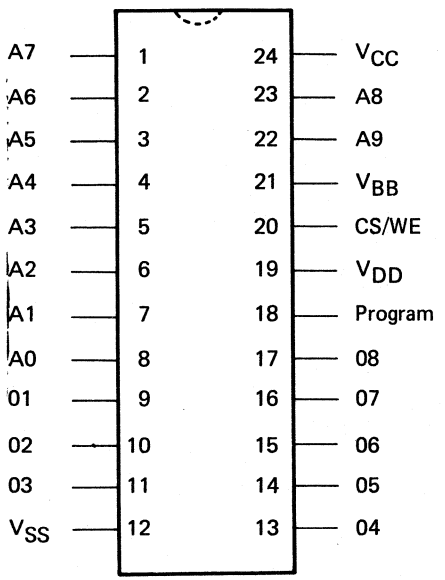


Figure 1. **MM**2708 PIN CONFIGURATION.

A0 – A8 Address Inputs

01 – 08 Data Outputs

CS/WE CHIP Select/Write Enable

4

The program pin (18) receives 26V pulses during programming **and** must be held at Vss (GND) or below V_{IL} during read operations. The cs/WE pin (20), serves the following three functions:

(i) When at V_{IL} (OV), the device is selected for normal read operation.

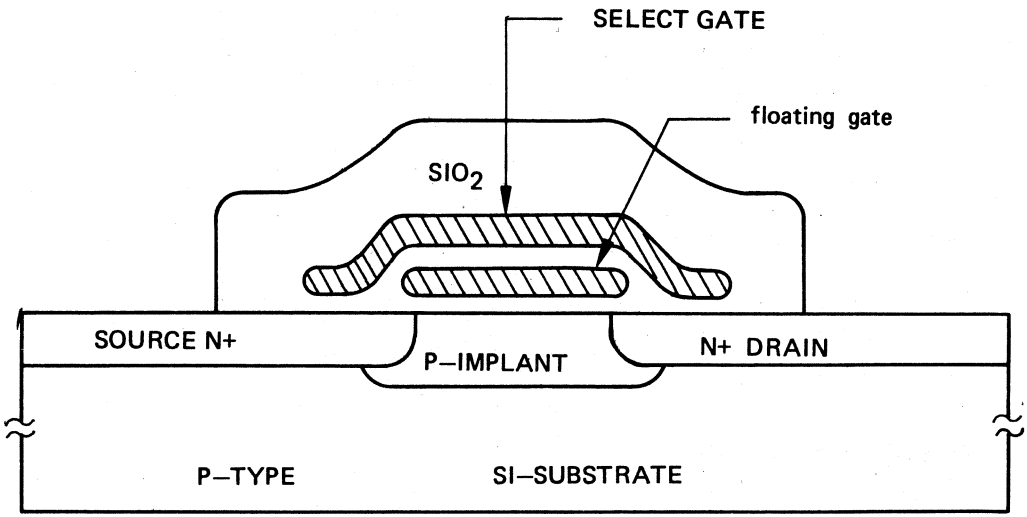
(ii) When at V_{IH} (3.0V, Min), the device is deselected and the outputs are placed in the high impedance state.

(iii) When at V_{IHW} (11.4V, Min), the device is write enabled and ready to receive program pulses.

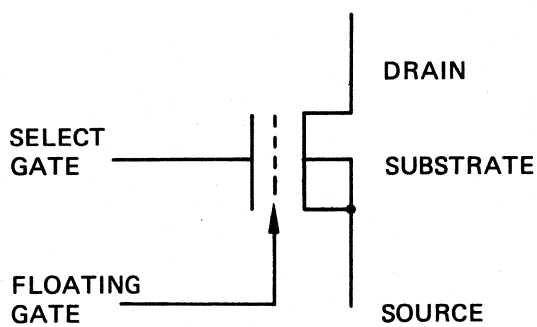
The low-order address bits (A0–A3) perform column (or Y) selection, while the high-order address bits (A4–A9) perform the row (or X) selection.

2.1 BASIC CELL

The storage medium of the National 2708 is a single transistor stacked-gate cell, implemented with two layers of polycrystalline silicon. The cell consists of a blottom floating gate and a top select gate, as shown in Figure 2. The top gate is connected to the row decoder, while the floating gate is used for charge storage. Both the first and second gate oxides are of standard production thickness, and the channel doping level is adjusted via ion implantation. The cell is programmed by injection of high energy electrons through the oxide, onto the floating gate. Once trapped- the charge remains there, as there are no electrical connections to the floating gate. The presence of charge on the floating gate causes a shift of the cell threshold voltage as shown in Figure 3.



(a) CROSS SECTION



(b) SCHEMATIC SYMBOL

FIGURE 2. MM2708 STORAGE CELL

FIGURE 2. MM2708 STORAGE CELL

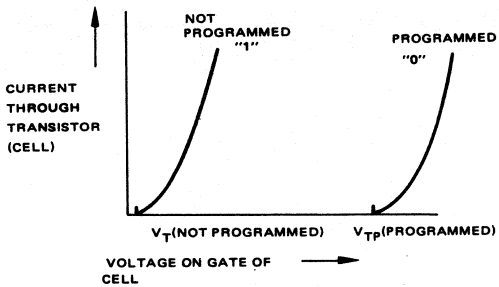


FIGURE 3. STORAGE CELL THRESHOLD SHIFT

In the initial state, when there is no charge on the floating gate, the cell has a low threshold and selection of the cell, by applying voltage on top select gate turns it on. But when programmed, the cell stores charge on the floating gate, and its threshold shifts to a higher level so that it will not turn on when selected.

2.2 ERASURE

As there are no electrical connections tl the floating gate, therefore stored charge in the cell must be removed by non-electrical means. Illumination of the cell with ultraviolet light of the correct wave length (2537A°) and energy (10 watt seconds/cm²) will impart sufficient photon energy to the trapped electrons to allow the floating gate to be fully discharged.

3. RELIABILITY

This section describes the tests conducted to establish the device reliability and as well as failure mechanisms involved. The following tests focus on charge loss characteristics and long term degradation.

(i) High temperature data rentention bake.

(ii) Dynamic high temperature life test.

In addition, several other tests such as activation energy experiments, programming margin, voltage SHMOO, prolonged erasure and multiple program/erase tests are currently in progress. This report will be updated with results from those tests as they become available.

3.1 DATA RETENTION

Data retention in the MM2708 was evaluated using high temperature bakes. A bit pattern was selected to program 'EPROM' cells and stored at high temperature (300 °C) to accelerate charge leakage from the floating gates. The cumulative percent failures then plotted with time for given bake temperature. Figure 4 shows the data retention characteristics of National 2708 at 300 °C in comparison with familiar P-channel EPROM, 1702A.

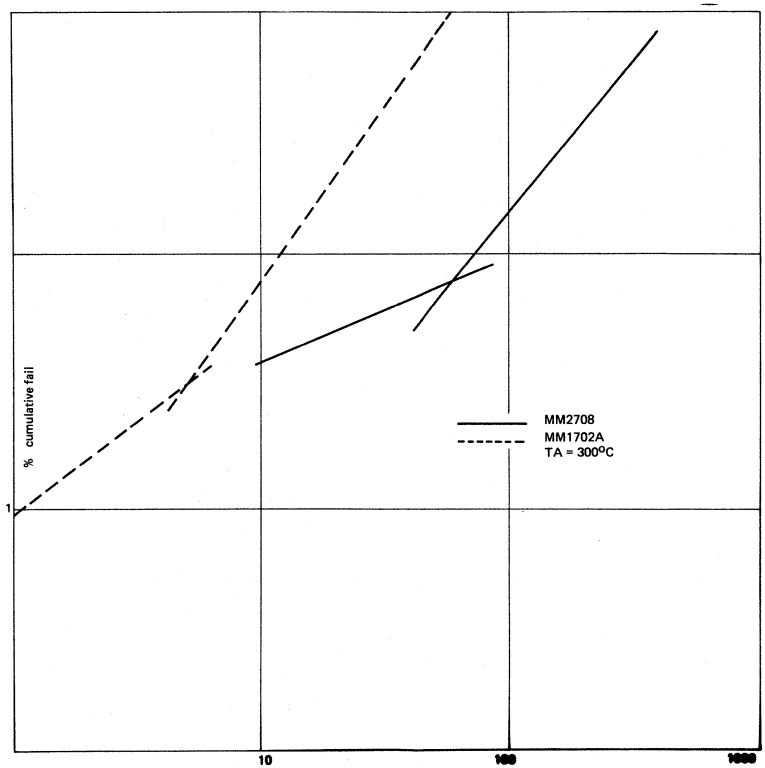


FIGURE 4 DATA RETENTION CHARACTERISTICS

3.2 LIFE TEST

This is a high temperature (125 °C) dynamic operating life test to stress the device in order to accelerate its failure mechanisms. The timing and voltage conditions are detailed in drawing No. 1310RE and the data obtained is summarized in Table 1. The failure rate predictions at 50 °C are given in Table 2.

SAMPLE SIZE	DEVICE HOURS	TA (°C)	NO. OF FAIL	FAILURE MODE
24	48,384	125	2	CHARGE LOSS
24	36,288	125	0	
48	72,576	125	0	

TABLE 1. DYNAMIC LIFE TEST DATA

TOTAL DEVICE HOURS AT 125 °C	EQUIVALENT DEVICE HOURS (0.7ev)	NO. OF FAIL	FAILURE RATE © 60% Conf. level	© 90% Conf. level
157,248	1.792×10^7 (50 °C)	2	.017%/khr	.029%/khr

TABLE 2. DYNAMIC LIFE TEST FAILURE RATES.

National Semiconductor

RELIABILITY REPORT M-40
MM5203Q
MOS 2048-BIT
ELECTRICALLY PROGRAMMABLE
READ-ONLY MEMORY
IN 24 LEAD QUARTZ LID
PACKAGE

SUMMARY

Samples of MM5203Q with quartz lids have been programmed with a customers program and have passed 1000 hours of High Temperature Operating Life Testing.

There were no failures. Based on the Arrhenius model (attached report G-11), the calculated failure rate at 70°C is 0.029%/1000 hours with a 60% confidence level.

D. Tovar
MOS Reliability

R. Kramer
Mgr. Reliability Assurance

ABSTRACT

M5203Q are at an acceptable reliability level of 0.029%/1000 hours at 70 °C (60% confidence level), with respect to HTOpL testing.

PURPOSE OF TEST

The purpose of this test was to use a customers program on Approved Box Stock drawn MM5203Q devices subject to HTOpL testing and electrically test for data retention.

SAMPLE DESCRIPTION

The MM5203Q is a 2048-Bit static read- only memory which is electrically programmable and uses solicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256 x 8-Bit words or 512 x 4-Bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

Twenty-eight (28 devices), MM5203Q, 24 lead, quartz lid version (which is erasable with short ultra-violet light, i.e., 253.7 n.m.) d/c 445, drawn from Approved Box Stock.

TEST DESCRIPTION

1. Test on Data 1/0 programmer, Model 1, for all "O"s.
2. Program all "1"s on Data 1/0 Programmer at 25 °C.
3. Test for all "1"s.
4. Erase for 20 minutes with ultra-violet light (253.7 n.m.).
5. Test for all "O"s.
6. Program all parts with "ATV" on Data 1/0 Programmer and verify.
7. High Temp Reverse Bias, $T_A = +125$ °C, $V_{DD} = +18V$ on pins 12, 16, 23, 24. All other pins are set to Vss per attached diagram.
8. Test on DAta 1/0 for "ATV" program retention at 0,168, 500 & 1000 hours data point.

Initially, all 2048 bits of the MM5203Q are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. Negative logic is used during the programming mode for data in. A "1" or a "P" at a data input corresponds to V_{ILP} A "O" or an N at a data input corresponds to V_{IHP}.

Word address selection is done by the same decoding circuitry used in the READ mode. The eight output terminals are used as data inputs to determine the information patern in the eight bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

Positive logic is used during the read mode for adresses and data out. Address O corresponds to all address inputs at V_{IL} and address 255_{IO} corresponds to all address inputs at V_{IH}. A "I" or a P at data output corresponds to V_{OH}. A "O" or an N at a data putput corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address O corresponds to all address inputs at V_{ILP} and address 255_{IO} corresponds to all address inputs at V_{IHP}.

A custom program has been chosen which randomly programs "O"s and "1"s into each word. In this manner, any programming interference of adjacent cells may be detected. The chosen program is pattern "ATV".

TEST RESULTS

1. All 28 pcs passed all "O"s testing.
2. All 28 pcs programmed with all "1"s.
3. All 28 pcs passed all "1"s.
4. All 28 pcs erased within 20 minutes.
5. All 28 pcs passed all "O"s testing.
6. All 28 pcs programmed with "ATV" and verified.
7. Test

Device	Qty	0	168	500	1000
HTOpL MM5203Q	28	0/28	0/28	0/28	0/28

There were no failures after 1000 hrs of HTOpL testing. Total unit-hours at $T_A + 125$ °C = 28,000, + 70 °C to + 125 °C acceleration factor (Figure A, Pg 4, G11) = 125X.

Total unit-hours at $T_A = 70$ °C = 3,500,000
Calculated failure rate at 70 °C with a 60% confidence level = 0.029%/1000 hrs.

CONCLUSION

Programmed MM5203Q are at an acceptable reliability level.